A STUDY ON DESIGN METHODOLOGIES OF POWER AMPLIFIERS USING SIGE HBT BICMOS TECHNOLOGIES

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A STUDY ON DESIGN METHODOLOGIES OF POWER AMPLIFIERS USING SIGE HBT BICMOS TECHNOLOGIES

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To my family

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SUMMARY

The goal of the proposed research is to develop multiple design methodologies of power amplifiers (PAs) using silicon germanium (SiGe) heterojunction bipolar junction transistor (HBT) to achieve highly efficient, high power, highly linear, and/or broadband amplification. Choosing optimal design method depending upon applications will be critical to overcome performance limitations imposed by the inherent low bandgap of SiGe HBT. This work provides several design examples of SiGe HBT PAs and explains design approaches suitable for each PA application by focusing on unique features of SiGe HBT devices for the large signal operation and by devising novel passive and active circuit design techniques. The following is the summary of this work.

1. The design of X-band inverse class-F PAs in advanced SiGe BiCMOS technology: The comparisons between the two PAs are made by selecting SiGe HBT device topology tailored for the high voltage swing operation and by developing several output passive networks to support inverse class-F mode. Those works had been accepted to IEEE Radio Frequency Integrated Circuits Symposium in 2017 [4] and IEEE Transactions on Circuits and Systems-II Express Brief in 2018 [58].
2. The co-optimized design of an asymmetric bulk CMOS SPDT together with a SiGe HBT cascode LNA: Simultaneous achievement of the low noise figure in the receive mode and the high output power handling ability in the transmit mode shows that the proposed co-design of X-band front-end-module (FEM)

can be promising in the implementation of low cost X-band phased arrays. This work was accepted in IEEE International Microwave Symposium in 2016 [71].

3. The design of an innovative passive circuit to realize a compact, low loss, and broadband lumped-element power divider and combiner: Subsequently, a design method of the SiGe HBT cascode non-uniform distributed power amplifier (NDPA) is proposed. With the improved lumped-element power divider and combiner, the NDPA achieves the output power level that is close to sub-Watt and very broad bandwidth at the same time. Those works had been accepted in IEEE Microwave and Wireless Components Letter in 2017 [77] and submitted to IEEE Custom Integrated and Circuits Conference in 2019.
4. The design of a highly linear SiGe HBT power amplifier supporting 802.11ac/11ax WLAN standards: A compact, 2nd harmonic-shorted four-way output transformer balun is proposed to increase its linear output power. A thermally compensated dynamic bias circuit is proposed in order to mitigate the electro-thermal effect in the design, which is a key circuit component in implementing highly linear WLAN PAs. This work had been accepted in IEEE International Solid-State Circuits Conference in 2019.
5. The design of a highly efficient, high power Ka-band frequency doubler for an emerging 5G wireless communication: A novel common-centroid layout technique and a four-way input transformer are proposed. The results of the proposed Ka-band SiGe HBT frequency doubler can be one of the key building elements of the 5G phased array transceivers. This work had been accepted in IEEE Transactions on Microwave Theory and Techniques in 2018 [56].

CHAPTER 1. INTRODUCTION

1.1 Origin and History of Problem

Wireless communication has long evolved with increasing demand on high data throughput access. It is important to develop low cost, high performance radio frequency (RF), microwave, or millimeter (MM-wave) transceivers. A power amplifier (PA), an electronic circuit that increases a magnitude of a signal by an amplification, is an essential component in a wireless transmitter due to its large power dissipation and inherent nonlinearity caused by a high voltage swing operation. As most of DC power is dissipated as heat, PA would be vulnerable to thermally induced electrical performance degradation and device breakdown. The most critical factor in designing PAs is their high voltage swing and large current operation, which always bring about the long-term reliability issue for mass production.

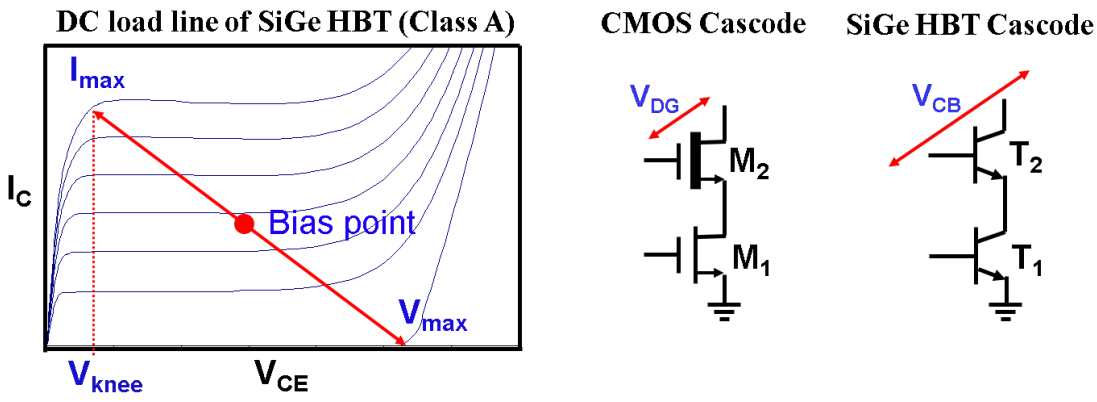
All those issues must be taken into account in PA design and that is why III-V compound semiconductor technologies, such as GaAs or GaN [1], have dominated in the development of PAs. Their very high breakdown voltage and superior speed make them attractive choice for designing cellular handset PAs and base station PAs at the cost of lower yields and limited availability of digital control functionality.

To replace expensive III-V processes with lower cost Si-based technologies such as complimentary metal-oxide-semiconductor field effect transistor (CMOS) or silicon-germanium (SiGe) heterojunction bipolar transistor (HBT), careful design methodologies should be developed not only by proposing novel circuit design techniques, but also by

accurate understanding of device physics to overcome performance limitation. The main reason is that requirements in a PA are clearly different depending upon its application; for wireless local area network (WLAN), in-band linearity of PAs is the most important metric while maximizing an output power (P_{OUT}) with a high power-added efficiency (PAE) are the most significant parameters of PAs for implementing low cost X-band phased array. The focus of this study are to clarify large signal characteristics of SiGe HBTs, understand electrical-thermal effects in SiGe HBTs, and develop several circuit design techniques for optimizing SiGe HBT PAs relied upon their applications.

1.2 Silicon-Based Transistor Technologies for Power Amplifier Design

It is widely known that the scale down of Si-based transistors over past decades has improved RF performance rapidly. As a result, the unity gain frequency (f_T) and the maximum oscillation frequency (f_{max}) of some Si-based transistors exceed 300 GHz and 500 GHz for CMOS [2] and SiGe HBT [3], respectively. Although this aggressive scaling can be beneficial for a high speed operation, it results in the unavoidable breakdown voltage reduction. This fundamental trade-off between the speed and the large signal operation is referred to as 'Johnson limit'. Therefore, it is fair to say that the Si-based PA design becomes more challenging as the operation frequency of devices increases. The inherent low bandgap of CMOS and SiGe HBT compared to their III-V counterparts further restricts the maximum voltage swing of CMOS and SiGe HBT transistors, which eventually impedes the design of high power and highly efficient Si-based PAs. Figure 1 plots the DC load line of a transistor operating in the class-A mode. P_{OUT} and PAE were obtained based on the following Equation 1 and 2. These equations show that the large voltage swing operation is the key to improving PA performance. Due to the high tolerance



(a) (b) (c)

Figure 1 – (a) DC load line of a SiGe HBT in class-A mode and circuit schematic of (b) CMOS cascode and (c) SiGe HBT cascode.

$$P_{OUT} = \frac{(V_{max} - V_{knee}) \cdot I_{max}}{8} \tag{1}$$

$$PAE = \frac{1}{2} \cdot \frac{V_{max} - V_{knee}}{V_{max} + V_{knee}} \cdot (1 - \frac{1}{G}) \tag{2}$$

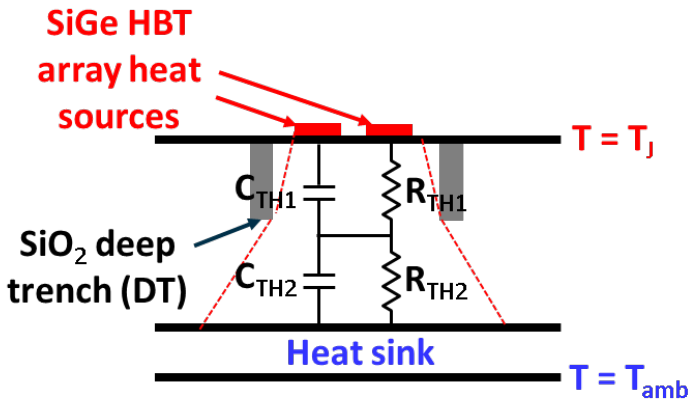
to a large voltage swing and its nature of reducing the Miller effect, the cascode topology is frequently utilized for power cell design in Si-based PAs. Figure 1 (b) and Figure 1 (c) show the simplified circuit schematics of both the CMOS cascode and SiGe HBT cascode. The figures show that they are identical in structure, however, there is a significant performance difference between them in the large signal operation. The CMOS gate oxide is inherently vulnerable to the breakdown. Under the large voltage stress, the gate-drain oxide of M_2 in the CMOS cascode is likely to be damaged, eventually shorting the gate and the channel of the transistor and results in a catastrophic damage. Therefore, the choice of M_2 often becomes a thick oxide device for the CMOS cascode for the higher voltage swing applications, at the cost of the reduction in f_T and PAE degradation. In general, the SiGe

HBT cascode has the higher voltage headroom than the CMOS cascade; its breakdown voltage depends strongly upon both a base impedance termination and a voltage-current waveform overlap [4]. The low impedance termination at base of the upper SiGe HBT (T_2) in the cascode helps route the impact ionization-induced excessive holes to ac ground, not flowing into its emitter. Thus, the voltage swing of the upper SiGe HBT can be higher than BV_{CEO} and is extended to BV_{CBO} if its dynamic voltage and current swing overlap is minimized. The SiGe HBT also endures the higher current density than CMOS does with the similar active area. In other words, SiGe HBTs have the smaller parasitic capacitance than CMOS at the similar speed of operation. Due to the superior large signal characteristics and the small input capacitance, the SiGe HBT cascode is favored in designing broadband distributed PAs [5].

It is important to note that the SiGe HBT cascode topology is not preferred selection in the linear PA design since the variation of the drain-to-gate capacitance of M_2 and the collector-to-base capacitance of T_2 under a high output voltage swing will cause both the amplitude to amplitude (AM-AM) and the amplitude to phase (AM-PM) conversion, which will greatly distort a modulated signal [6, 7]. Thus, the common-source (CS) or common-emitter (CE) transistors are better choices for the linear PA design if the devices are not subject to the high voltage stress.

This unique high voltage operation capability of SiGe HBTs is the main reason that they are preferred over CMOS in implementing the high performance and reliable PAs at the comparable cost. In this study, the large signal excursion of SiGe HBTs is demonstrated by the highly efficient X-band PAs, a broadband distributed PA, a highly linear WLAN PAs, and Ka-band frequency doubler, all of which are designed utilizing SiGe HBTs.

1.3 Electro-Thermal Effect of SiGe HBT



	Thermal conductivity (W/cm°K)
SiO_2	0.014
Si	1.54
GaAs	0.52

Figure 2 – Cross-section of a SiGe HBT with a simplified thermal equivalent circuit and thermal conductivity of various materials.

As stated in the previous section, SiGe HBT technology is advantageous over CMOS for PA design for its capability to handle higher voltage swing, higher current swing, and thus larger power density. However, the effects of device self- and mutual-heating become increasingly significant as power density increases. For the same amount of power generated, power cells using SiGe HBTs have smaller volume for heat dissipation to a backside heat sink than CMOS power cells with smaller power density. This significantly effects on power cell electrical performance (current gain (β) drop and f_T/f_{max} reduction) and long-term reliability [8]. The junction temperature (T_j) of a SiGe HBT increases as it dissipates power as heat, an effect referred to as self-heating. Figure 2 depicts a simplified cross-section of a SiGe HBT. Since the thermal conductivity of Silicon (Si) is much higher than that of the substrate material of III-V platforms, such as GaAs, one would expect SiGe HBT devices to be superior compared the III-V counterpart in term of thermal property. For better electrical isolation, modern SiGe BiCMOS platforms usually include SiO_2 deep trenches (DT) around active regions [9]. Since a SiO_2 DT is very good thermal insulator,

it will hinder heat flow from the active devices to the backside heat sink, increasing T_j of SiGe HBTs. Effectively, the area for the thermal dissipation is reduced due to the existence of the DT. The measure of heat dissipation capability is modeled using thermal resistance (R_{TH}), defined as T_j increase per power dissipated as heat. Thus, it is easily anticipated from Figure 2 that R_{TH1} is higher than R_{TH2} because of the effectively smaller area of the region where SiO_2 DT exists. In PA design, the accurate model of thermal resistance is important to simulate the performance change due to thermal effects [10-12].

To model the time delay for the T_j of a power cell to reach its thermally steady state, a thermal capacitance (C_{TH}) is added in parallel with R_{TH}, and hence defines a thermal time constant ($\tau_{TH} = R_{TH}C_{TH}$). τ_{TH} is the amount of time it takes to heat up a specified volume of material to 63.2% of the steady state temperature. Details on how this thermal transient effect is involved with PA's in-band nonlinearity will be treated in a chapter V.

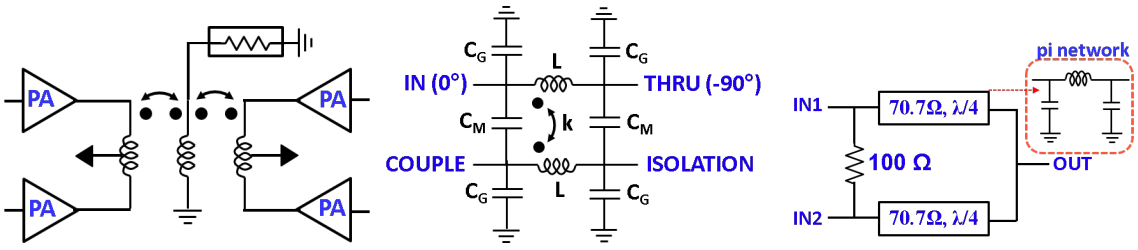
In Watt-level PA designs for modern wireless standard, a SiGe HBT array with multiple emitter stripes is preferred over a single-finger device for Si area saving and reduced parasitic. The use of multi-finger SiGe HBT power array, however, leads to further increase in T_j of the SiGe HBTs in the array due to mutual heating effect[13, 14]. Individual emitters at a multi-finger SiGe HBT array are thermally coupled through Si substrate because the emitter stripes are not thermally isolated by SiO_2 DT. With self-heating and mutual thermal coupling consideration, T_j of each finger in a SiGe HBT array is as below.

$$\boldsymbol{T_{j(i)} = T_{AMB} + R_{TH(ii)} \cdot P_{D(i)} + \sum_{j=1}^{n} R_{TH(ij)} \cdot P_{D(j)} \quad where\ i \neq j} \qquad (3)$$

where $T_{j(i)}$ is a junction temperature of *ith* finger in the HBT array, T_{AMB} is an ambient temperature of the SiGe HBT array, $R_{TH(ii)}$ is a self-heating thermal resistance of *ith* finger, $R_{TH(ij)}$ is a mutual thermal resistance of *ith* finger by the power dissipation in the *jth* finger, and $P_{D(i)}$ and $P_{D(j)}$ are power dissipated in the *ith* and the *jth* fingers, respectively. There have been extensive studies on the mutual thermal coupling effects in literature by modeling $R_{TH(ij)}$ with various SiGe HBT geometries. Mutual heating is a significant contributor to T_j rise, leading to PA's electrical performance degradation and causing long-term reliability issue. From Equation 3, it is easy to see that the emitter stripe at the center of SiGe HBT array will have the highest junction temperature if each finger dissipates same power as heat. If this effect is getting worse, a most of collector current of the SiGe HBT array flows through the emitter stripe at the center and eventually the device will be damaged permanently. This positive thermal-electrical feedback effect is referred to as "thermal-runway". To address this current hogging effect, researchers have proposed multiple SiGe HBT power array layout techniques by varying spacing between emitter stripes [15], employing emitter ballasting resistors with non-uniform values [16], and using different emitter length for each finger in the array [9]. All of above scheme is to achieve a uniform temperature distribution on the SiGe HBT array for better electrical performance and reliable operation, at the cost of Si die area.

Therefore, it is essential for PA designers to understand how the electrical-thermal feedback affects the overall performance of the PAs, and to find methods to reduce the thermal effect in the PA operation. In the proposed research, the details of a linear, high power 802.11ac/ax WLAN SiGe HBT PA design methodology is proposed by designing a thermally-compensated dynamic bias circuit with the aid of layout-based thermal model.

1.4 Power Combiners and Power Cell Configurations



(a) (b) (c)

Figure 3 – Simplified circuit schematics of (a) a 4-way transformer, (b) a lumped-element quadrature hybrid, and (c) a lumped-element Wilkinson power combiner.

Many groups have been focusing on increasing the output power either by devising various types of power combiners or transistor configurations. An on-chip transformer balun [17] is very popular for implementing differential PAs because it can be exploited as an impedance converter, a single-ended to differential conversion or vice versa, a RF choke for biasing, and the most importantly, a power combiner. There are many design factors of integrated transformers including quality factors of primary and secondary windings, a magnetic coupling coefficient between them, inter-winding parasitic capacitances, and parasitic capacitances to a lossy Si substrate. [17-19] models on-chip transformers using lumped-elements but its accuracy is limited to low frequency bands and thus EM-based simulation provides the best accuracy.

The number of power cells that an on-chip transformer combines is from two to four or even to eight. A two-way transformer balun [20] is the most frequently used power combiner, especially in CMOS PAs, since its differential nature creates virtual ground at all common node in the circuit. As a result, wire-bonding parasitic inductance at a common source node of a CMOS differential pair has no impact on its power gain characteristic.

The first development of 8-way transformer is the distributed active transformer architecture [21]. As operating frequency increases the 8-way transformer structure is hard to be used as a power combiner due to complicated layout for routing and a large mismatch caused by inter-winding parasitic capacitances. Figure 3 (a) shows a circuit schematic of a four-way transformer [22]. It can be realized within a single inductor footprint with relatively simple signal routing. In addition, some attractive features provided by the four-way transformer leaves a design space for improving the performance of PAs. In this study, several types of transformers are proposed and used as power combiners, harmonic impedance synthesizer for waveform engineering, and a power splitter.

Figure 3 (b) indicates a circuit schematic of a lumped-element quadrature hybrid [23, 24]. Two inputs (IN and THRU) with 90° phase shift are combined in phase at "COUPLE" port with high isolation at "ISOLATION" port. This type of the power combiner is compact and low loss, but its bandwidth is usually limited to 10~20%.

For a single-ended configuration, Wilkinson power divider/combiner (WPDC) is used for power splitting and combining due to its low loss, high isolation, and robustness to mismatch caused by process variation [25, 26]. The requirement of at least two λ/4 impedance transformers (usually realized in microstrip T/Ls) would occupy large Si area and thus not appropriate as an on-chip power combiner. In order to fully take advantage of its beautiful properties and reducing Si-area consumption at the same time, a lumped-element artificial λ/4 transformer is adopted to the WPDC [27, 28]. The design example is shown in Figure 3 (c). The disadvantage of the lumped-element WPDC, however, stems from a low cutoff frequency of a pi-network. The proposed research would resolve the

bandwidth limitation of the lumped-element λ/4 transformer by using a novel layout technique and apply it to a broadband SiGe HBT cascode distributed PA design.

Stacking multiple transistors in series [29-31] as power cells in a PA are spotlighted as one viable methodology since it enables to increase supply voltage without device breakdown and obtain optimum impedance close to 50Ω for wideband operation. By terminating proper value of a bypass capacitor at each gate/base of a stacked transistor with optimized gate/base bias voltages, a voltage swing between gate/base to drain/collector of FET/HBT can be reduced and thus it helps to avoid the device breakdown. There are two limitations, however, in increasing the number of stacked transistors; one of which is that the required bypass capacitor is getting extremely small as the number of stacking increases and thus hard to realize it precisely. Another is a phase misalignment of voltage swings at drain/collectors of transistors induced by a parasitic capacitance at an intermediate node between two transistors, which degrades both P_{OUT} and PAE. As a result, the number of transistor stacking is empirically limited to 3 or 4. One more design issue of stacked PAs using SiGe HBT is a finite base current. As mentioned, upper HBTs in the stacked PA requires a small value of capacitor, meaning a very high series bias resistor must be inserted to decouple the ac voltage swing at the base of a SiGe HBT from DC supply. With P_{OUT} increase, the large voltage drop through the series resistor would require the use of higher base bias than a supply voltage at the output of the stacked SiGe HBT PA. In system perspective, it requires a DC-DC converter that drops the voltage further, resulting in efficiency degradation [32]. In this study, stacked SiGe HBTs are not applied to any SiGe HBT PA design. Instead of it, a common-emitter SiGe HBT and a cascode SiGe HBT are exploited for a linear PA and highly efficient/broadband PAs, respectively.

1.5 Development of Front-End-Module (FEM)

As a PA operates with other circuit blocks, such as a low noise amplifier (LNA) and a single pole double throw switch (SPDT), the co-optimization among them becomes critical. The integration of the PA, LNA, and SPDT in a single package is referred to as "Front-end-module (FEM)". The role of FEMs is becoming more crucial since many wireless communication standards, such as WLAN, 4G LTE, and phased array radar systems, operate under the time division duplex (TDD) mode. In TDD mode, the alternative turning on and off between the PA and LNA through the SPDT enables sharing the same antenna, which helps to reduce the size of the transceiver and remove a lossy and bulky frequency duplexer used to suppress the leakage signal from the PA to LNA.

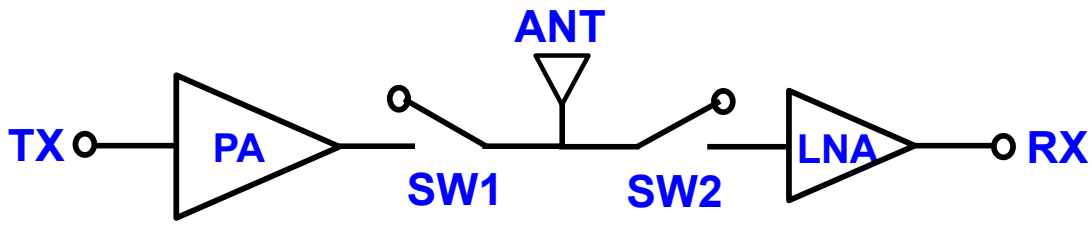


Figure 4 – Block diagram of a wireless front-end-module (FEM).

Figure 4 shows the simplified block diagram of the FEM that consists of PA, LNA, SPDT (SW1/SW2), and a single antenna (ANT). The co-optimization of the FEM heavily depends upon how the SPDT that bridges between the PA and the LNA is designed properly. There are multiple design parameters of the SPDT including the insertion loss (IL), isolation (ISO), return loss (RL), 1 dB compression power point (P1dB), and the 3rd order intercept point (IIP3/OIP3). These parameters are important to maintain the output power of a PA high and to keep noise figure of a LNA low.

The deep N-well NMOS with the floating body technique [33] is the most popular scheme to realize the highly linear SPDTs. The major difficulty in realizing SPDTs comes from the unavoidable tradeoff among the IL, the ISO, and the linearity. In order to decrease the IL for P_{OUT} of the PA and the noise figure (NF) of the LNA, a short channel length NMOS is used at the expense of the reduction in the breakdown voltage, which will restrict the power handling capability. If a wide gate width NMOS is used for a switch design to reduce its on-resistance (R_{ON}), it results in the increase of parasitic capacitance and the RF signal leakage. In order to obtain both the low IL and good linearity, [34] applied the negative bias to the body of NMOS to prevent the parasitic source/drain junction diode from turning on when the voltage swing is high. But generating the negative bias makes the entire system complicated, therefore, not a recommended option for integration.

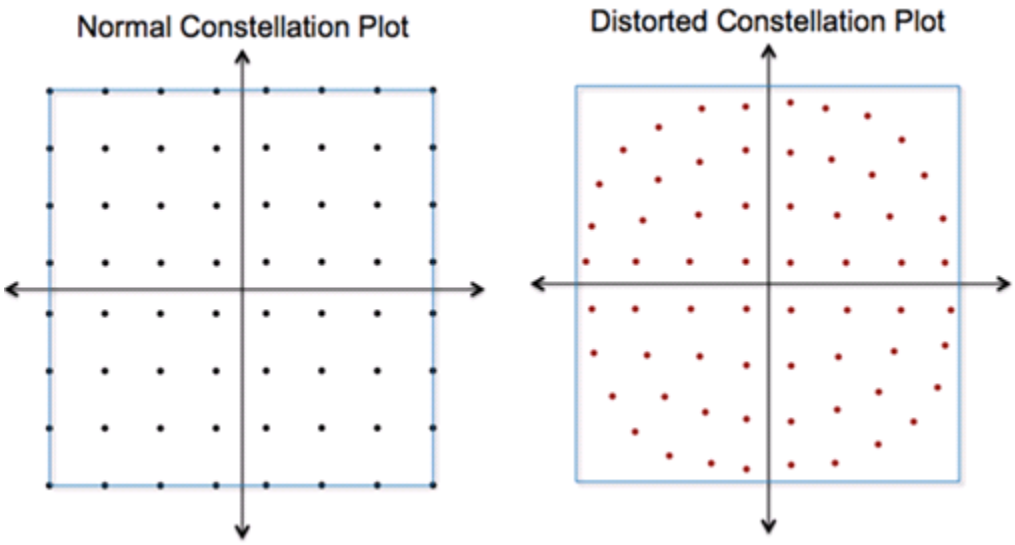
To obtain the high ISO between the transmit path (PA-SW1) and the receive path (SW2-LNA), the series-shunt SPDT topology is utilized. Multiple FETs in series are used on the series and the shunt branches of the SPDT to maintain the linearity at the high power operation. In order to gain the high ISO and good linearity, the R_{ON} of a shunt switch must be reduced, which implies that the large periphery NMOS need to be employed. This requirement also increases the parasitic capacitance of the NMOS switch and decreases the off-resistance, eventually, resulting in the IL degradation.

To resolve these trade-offs, the Silicon-on-Insulator (SOI) CMOS [35] has been utilized for the SPDT design. The SOI FETs have the significantly reduced junction diode capacitance compared to the regular FETs (i.e., non-SOI), which allows designers to use the wide gate width FETs in series to attain both the low R_{ON} and the reliability under a large voltage swing. Therefore, most commercial SPDTs are fabricated using SOI CMOS

technologies. However, the existence of the SiO_2 insulator underneath the active region of NMOS transistor hinders the thermal flow toward the backside heat sink; this phenomenon is equivalent to a thermal resistance increase and would be detrimental to PAs. The thermal dissipation issues in the SOI CMOS force designers to integrate the PA, LNA, and SPDT onto multi-chip modules (MCM) [36] using different technologies, but the package interface design can be complicated resulting in the manufacturing cost rise.

In this work, an optimized design methodology of the high power handling CMOS SPDT and an ultra-low noise SiGe HBT cascode LNA for the X-band FEM that mitigates the effects of the thermally susceptible SOI CMOS process is proposed.

1.6 Linear PA Design Using Si-based Technologies



(a) (b)

Figure 5 – Constellation of 64QAM signal without (a) distortion and (b) with distortion.

To deliver more information within a limited available spectrum, both amplitude and phase in a waveform are modulated. Quadrature amplitude modulation (QAM) is the most

widely used modulation scheme in modern wireless communication. Depending upon the number of bits in a symbol, the concept of QAM is extended to denser constellations. For example, 802.11n WLAN standard uses 64QAM (six consecutive bits in a binary baseband stream) that theoretically supports a maximum data rate of 54Mb/s in door wireless communication. Figure 5 shows a signal constellation of 64QAM with and without distortion in amplitude and phase. The constellation provides a quantitative measure of the signal distortion. The deviation from their ideal locations on the constellation is referred to as "error vector magnitude (EVM)" [37]. For a signal integrity, PA must be a highly linear, that is, the PA should be able to amplify the modulated signal with minimized amplitude and phase distortion.

Unfortunately, a SiGe HBT has many nonlinear elements [7] such as C_{BE}, C_{BC}, transconductance (g_m), and an output resistance (r_o) that, together, cause amplitude and phase distortion under large signal operation. These in-band distortions, called amplitude-amplitude (AM-AM) conversion and amplitude-phase conversion (AM-PM), are closely involved with EVM performance of a PA. Because QAM signals exhibit large envelope variations, PA should not operate at near saturated output power (P_{SAT}), but at power back-off (PBO) by a couple of dBm. PBO level of a linear PA is higher if orthogonal frequency division multiplexing (OFDM) is applied to a modulated signal [38]. In PA design, peak-to-average power ratio (PAPR) is defined as the ratio of the highest power to the average value. It is an indicator of how much PBO is needed for PA to amplify a modulated signal linearly. The wider channel bandwidth of QAM signal requires the higher number of subcarriers in OFDM, leading to high PAPR. PBO up to 11 dB is necessary for 802.11ac WLAN standard, which imposes stringent linearity requirement on PAs. With such a high

PAPR, the operation of WLAN PAs at large PBO is necessary for linear amplification. As a result, both P_{OUT} and PAE degradation are unavoidable, which limits the wireless connection coverage and reduces battery life of PAs.

Other than the in-band nonlinearity, the out-of-band nonlinear effect, "spectral regrowth," is also undesirable. It is caused by third-order nonlinearity of a PA with a variable envelope signal and leaks power to the adjacent channels [39].

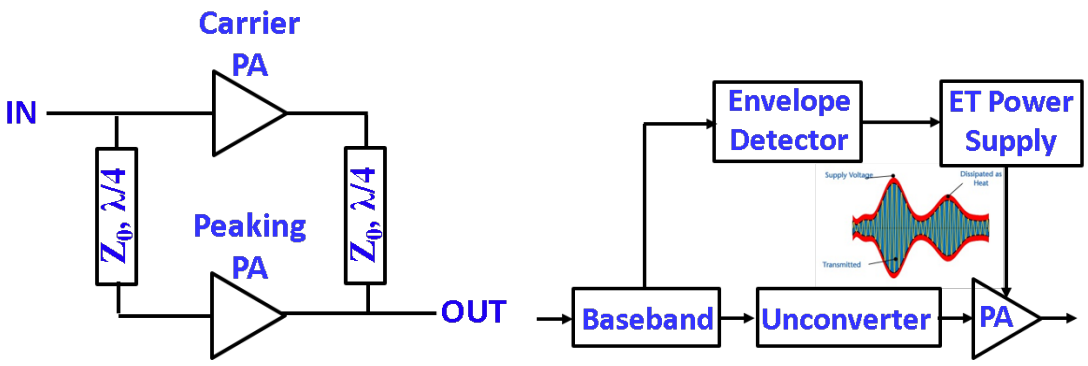
The importance of in-band and out-of-band nonlinearities strongly depends on PA applications. For indoor wireless connectivity like 802.11n/11ac WLAN, in-band linearity is more critical than out-of-band linearity due to very high EVM requirement and relatively low output power emission from a transmitter. For 4G LTE cellular wireless communication, however, out-of-band linearity is the dominant factor in determining quality-of-service wireless connection because the transmit output power and the number of users for LTE are higher than those for the indoor wireless connectivity solutions.

Various techniques have been developed to improve PA linearity. To reduce AM-PM distortion of a PA, a varactor-based capacitance compensation scheme is exploited in CMOS PA design [40]. A PMOS varactor with proper gate width is put at the gate of a common-source NMOS power cell transistor to compensate for the increase of its input capacitance with respect to increase in input power. This makes the overall input capacitance relatively constant with a variable envelope input signal, alleviating AM-PM. The disadvantage of this method is that the total input capacitance is about twice without the PMOS varactor compensation, which causes significant bandwidth reduction. Therefore, this technique is not suitable for wideband and high-power PA design.

A 2nd harmonic short termination at the output of transistors is a classic and effective way to improve both in-band and out-of-band linearity of PAs [41]. A 2nd harmonic current can be in phase with the fundamental current, leading to the increase of the peak voltage swing at the output of a transistor, limiting the maximum Pout at fundamental frequency and causing phase distortion. Out-of-band nonlinearity is also reduced by using the 2nd harmonic short trap since most of 3rd harmonic nonlinearity is induced by mixing between the fundamental and 2nd harmonic currents [42]. A series LC tank in close the output of a transistor is used as a 2nd harmonic trap. The main issue of applying the 2nd harmonic short termination to the PA is a tradeoff between bandwidth and performance. For wide bandwidth operation, a high capacitance value is needed for the 2nd harmonic LC tank, but this also increases a parasitic capacitance at the output of transistors, limiting the bandwidth of the PA at the fundamental frequency. Moreover, the 2nd harmonic trap occupies Si area and complicates signal routing, especially in a differential configuration. Therefore, careful design of schematic and layout is critical for optimizing linearity of PAs by using the 2nd harmonic short termination.

Digital pre-distortion (DPD) is one of promising linearization technique for PAs [43]. DPD is attractive in deep-scaled CMOS for its highly integration capability and reduced power consumption. If the PA nonlinearity is monitored using a feedback, it is possible to intentionally distort an input signal in a way that cancels the nonlinearity of the PA. This pre-distortion concept can be more robust if realized in digital domain. For example, if a small part of signal from a PA output (it contains both amplitude and phase nonlinearity information) is coupled to digital base band circuitry, the amplitude and phase of the baseband modulated signal are distorted to cancel the nonlinearity of the PA. This method,

however, is difficult to implement for wideband linear PA due to the requirement of the high speed DPD.



(a) (b)

Figure 6 – Conceptual block diagram of (a) Doherty PA and (b) envelope tracking PA.

Demands for PAs with high PBO efficiency introduced two representative design techniques; one of which is Doherty PA [44, 45] and another is envelope tracking (ET) PA [46, 47] . The former is based upon an active load modulation and the latter is based upon a supply modulation. Figure 6 shows their conceptual block diagrams.

The Doherty power amplifier is composed of a carrier amplifier, a peaking amplifier, and two λ/4 impedance transformers. Different operation classes between the two amplifiers and the impedance inverters enable to modulate an optimum load impedance at 6 dB PBO, which leads to higher efficiency than conventional linear class-AB PAs. The requirement of two λ/4 impedance transformers consumes large Si area, which induces significant loss at the output, and limits the operating bandwidth. The discontinuity at 6 dB PBO between the class-AB carrier amplifier and the class-C peaking amplifier would require careful gain and phase linearization through the DPD, which would complicate the Doherty PA design.

ET PA modulates drain/collector supply voltage of CMOS FET/SiGe HBT by tracking the input envelope variation, which results in a constant optimum impedance over a wide range of PBO. Unlike the Doherty PA, the ET PA does not require bulky impedance transformers and therefore it would be more compact. To achieve high efficiency operation at high/low power mode of operations, a high speed, highly efficient supply modulator design is critical. More specifically, the power supply modulator's bandwidth should be a few times wider than that of the modulated signal for tracking the input envelope quickly. It is reported from [46] that the supply modulator has bandwidth of 100 MHz for supporting 20 MHz LTE signal. The efficiency of the ET supply modulator is degraded at low voltage region due to a knee voltage of a transistor. In order to mitigate the knee voltage effect, an envelope shaping is carried out on the supply [48], which slows the supply reduction at the low input envelope signal. The gain reduction at low supply voltage is compensated by an adaptive bias [49]. As there is a fundamental tradeoff between speed and efficiency of the ET supply modulator, it would be hard to apply this scheme to wide bandwidth, linear PA design.

1.7 Spectral Purity Local Oscillator (LO) Signal Synthesis Using SiGe HBT

Rapid growth of data usage in modern wireless communication has been depleting available frequency resources quickly. Ka-band (28/39 GHz), once prevalently used for military and satellite communications, has recently been allocated for the next generation wireless standard and it is called fifth generation (5G) communication [50, 51]. With nearly unlimited access to information and data sharing with low latency thanks to a big chunk of the frequency spectrum, this emerging 5G wireless standard is going toward the final deployment.

For supporting data rates of 10 Gb/s with a given spectrum, a higher index modulation scheme such as QAM are utilized, but its modulation quality is very sensitive to a spectral purity of a local oscillator (LO) signal. Compared to RF bands, it will be very challenging to generate the low phase noise LO signal at millimeter-wave frequency bands. According to study [52], a flicker noise, also referred to as 1/f noise, is a dominant contributor to phase noise. Up-conversion of the flicker noise generates wide skirt power spectrum around a LO signal, which degrades the quality of modulated and demodulated signals. Due to the nature of the vertical current transport, the flicker noise of the SiGe HBT is much lower than that of a NMOS transistor (lateral current flow in the interface between Si and SiO_2) and thus the SiGe HBT is better solution to generate the low phase noise LO signal. Even with such desired property of the SiGe HBT, the low phase noise LO generation is getting difficult with a carrier frequency increase. Following Equation 4 [53] explains Lesson's phase noise model of oscillators and it is expressed as below

$$\mathcal{L}(\Delta\boldsymbol{\omega}) = \mathbf{10} \cdot \boldsymbol{log}\left[\boldsymbol{F}\frac{\boldsymbol{4kTR_p}}{\boldsymbol{V_p}^2}\frac{\boldsymbol{\omega_0^2}}{\boldsymbol{4Q^2\Delta\omega^2}}\right] \tag{4}$$

where Q is a quality factor of a LC tank, F is noise factor of an active device, V_p is an oscillation amplitude in the resonating LC tank, R_p is an equivalent parallel resistance of the LC tank, and $\Delta\omega$ is the delta frequency from the carrier frequency ω_0. Equation 4 indicates that the phase noise degradation is proportional to a square of ω_0, which is amount to 12 dB phase noise increase at twice ω_0. In addition, the Q of the LC tank will be decreasing at higher carrier frequency due to higher loss of inductors and varactor diodes, which further degrades phase noise. The large oscillation amplitude improves the phase

noise of oscillators, which inevitably requires use of high supply and brings about reliability issue. Thus, synthesizing an excellent spectral purity LO signal at MM-wave band is extremely difficult task.

One solution for mitigating the phase noise of a LO signal at higher frequency is to multiply a low frequency LO signal by using a frequency multiplier [54, 55]. Phase noise degradation factor is known as 20 x log(M), where M is a frequency multiplication factor. For example, if M = 4, the relative phase noise degradation between a LO signal source realized with a frequency quadrupler and that without the frequency multiplier is 12 dB if other degradation factors are assumed to be same. Among many types of frequency multipliers, frequency doublers [56, 57] would be popular due to their capability for high P_{OUT}, high conversion gain, and high efficiency. As 5G phased array will operate with multiple-input/multiple-out (MIMO) technique, the number of transmit and receive paths would be higher than 3G or 4G communications, which requires the higher LO power generation and distribution. Therefore, designing a Ka-band frequency doubler supporting high power and high efficiency operation would be one of key building block in 5G wireless transceiver design. In the proposed research, the design of a compact, highly efficient, and high power Ka-band SiGe HBT cascode frequency doubler is presented to surmount the performance of Si-based Ka-band frequency doublers reported to date.

1.8 Organization

The goal of this study is to demonstrate the capability of SiGe HBT BiCMOS technologies to develop optimal design methodologies tailored for power amplifiers. Several design examples are provided, which clearly show that SiGe HBTs can be utilized

to achieve the best performance, not only by proposing novel circuit techniques, but also by fully understanding the device characteristic of SiGe HBTs. The correlation between circuit and device design would be right direction to overcome the limitation imposed by the low bandgap Si-based transistors. Chapter II discusses the design of two types of highly efficient sub-Watt level X-band inverse class-F SiGe HBT cascode PAs and compare their performance. In Chapter III, a co-design method between a SiGe HBT cascode LNA and bulk CMOS FET SPDT is proposed for a low cost, high performance X-band phased array system. Chapter IV describes the motivation of a wideband wireless communication and proposes new lumped-element Wikinson power divider/combiner (WPDC). Subsequently, the design of a broadband sub-Watt level SiGe HBT cascode distributed PA is proposed based on further innovation in the WPDC and by developing a non-uniform distributed PA core with a lower load. In Chapter V, the design method of a highly linear, high power SiGe HBT PA for 802.11ac/ax WLAN standards is established by taking electrical-thermal effect into consideration in the design and propose a built-in 2nd harmonic-shorting four-way output transformer balun for linear amplification. Chapter VI describes a compact, highly efficient, and a high power Ka-band SiGe HBT cascode frequency doubler for emerging 5G communication. Finally, chapter VII reviews the results of the multiple design of SiGe HBT PAs and discuss future works based on the results.

CHAPTER 2. DESIGN OF SIGE HBT CASCODE INVERSE CLASS-F POWER AMPLIFIERS

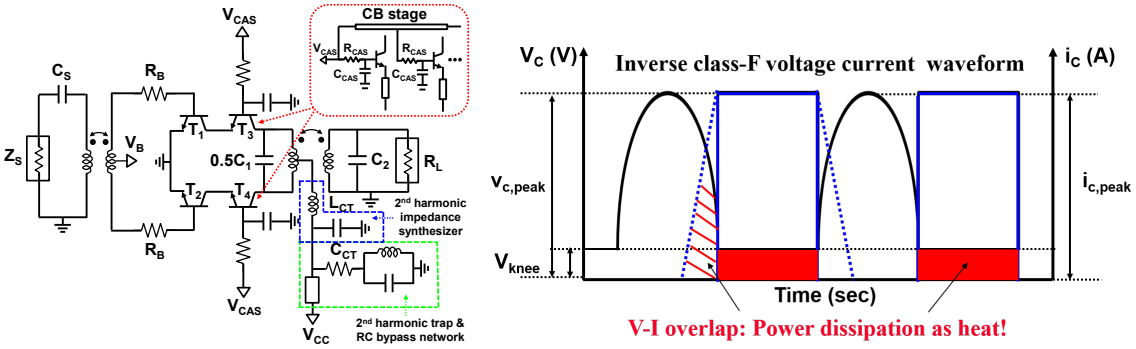
In this chapter, the design of two types of X-band PAs using SiGe HBT BiCMOS technology is studied in detail. At first, the large voltage excursion of SiGe HBT cascode is explained and inverse class-F operation is studied. Different passive design approach is adopted to realize the inverse-class F mode for highly efficient PA implementation. Finally, the comparison between the two is made which topology is more promising in the development of a multi-functional, low cost X-band phased array. Those works had been accepted to IEEE Radio Frequency Integrated Circuits Symposium in 2017 [4] and IEEE Transactions on Circuits and Systems-II Express Brief in 2018 [58].

2.1 Highly Efficient X-band SiGe HBT Cascode Inverse Class-F PA With Harmonic-Tuned Output Transformer Balun

With rapid scaling in transistors, Si-based technologies are being spotlighted for the development of X-band phased array due to their lower cost, higher yield, and denser integration compared with III-V compound processes. While SiGe HBT will be appropriate solution in implementing extremely low noise X-band receiver [59], it would be hard to realize Watt-level X-band PAs due to the inherent low breakdown voltage. The limitation on the large signal operation obstructs the design of high power, highly efficient X-band PAs. Thus, most of research have focused on improving the output power by exploiting power combiners and/or transistor stacking. But the improvement in the efficiency of SiGe HBT X-band PA is still at standstill and most of power is dissipated as heat, which would require complex thermal compensation bias circuits to prevent performance degradation.

Switching mode PAs have been widely investigated to achieve high output power and high efficiency concurrently. Those have been successfully designed at RF bands and are recently migrated to microwave and MM-wave bands. A class-E switching PA [60] obtained high efficiency with modest output power, but its performance is significantly limited by a parasitic capacitance of SiGe HBT. While an inverse class-D PA [61] is frequently used in RF band, it is not suited for use in X-band since they require square pulse shaping at input. The inverse class-F PA [62] represents a possible alternative for realizing highly efficient operation at microwave frequencies, but it has proven challenging to attain Watt-level output power due to the absence of power combining.

In this section, we demonstrated sub-Watt level highly efficient X-band inverse class-F PA by proposing a novel harmonic tuned output transformer balun and SiGe HBT cascode to maximize voltage swing. Figure 7 (a) shows the circuit schematic of the proposed PA. A differential topology is adopted to provides separate matching ability between odd- and even-modes, which facilitates the optimization of fundamental and 2nd harmonic impedance termination simultaneously. The PA is comprised of two cascode power cells with an input transformer balun and an output transformer. Both CE ($T_{1/2}$) and CB ($T_{3/4}$) are 7 HBTs in parallel with emitter width and length of 0.12 μm and 17.8 μm, respectively. Each unit cell has a total emitter area of 14.95 μm^2, decided to suppress Kirk effect at high current density. Red dotted box in the circuit schematic shows the detailed configuration of the CB transistor in cascode. The base of each SiGe HBT is terminated with a 1 pF high density high Q MIM capacitor C_{CAS} to bypass excessive holes generated by impact ionization. Series resistor R_B and a 2nd harmonic trap (green box as highlighted in the circuit schematic) were inserted to stabilize the PA.



(a) (b)

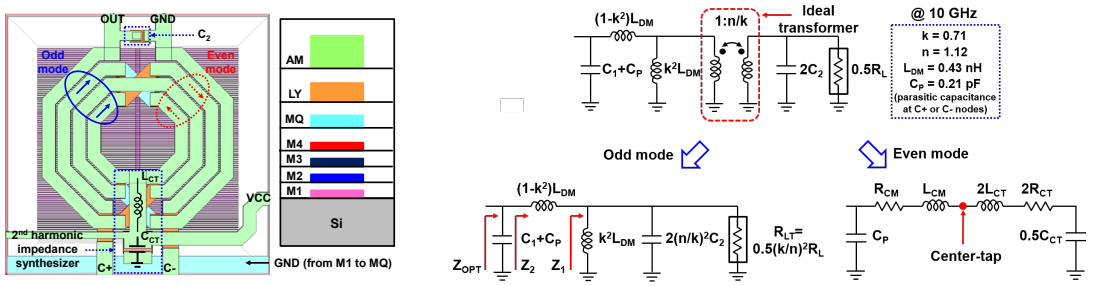
Figure 7 – (a) Circuit schematic of a X-band SiGe HBT cascode inverse-class F PA with a 2nd harmonic-tuned output transformer balun and (b) dynamic voltage and current waveforms of inverse class-F mode.

Inverse class F mode is a sort of waveform engineering, as shown in Figure 7 (b). Voltage is a half sinusoidal wave and current has square waveform. To support inverse class-F mode, impedance condition at harmonic frequencies must be as below

$$\boldsymbol{Z_{odd} = 0} \quad , \quad \boldsymbol{Z_{even} = \infty} \tag{5}$$

Equation 5 obtained based on Fourier series. In reality, it is very hard to satisfy open at all even harmonics and short at all odd harmonics, so most of works only synthesize 2nd/3rd harmonic impedances, which induces the voltage-current waveform overlap, eventually degrading efficiency. Also, a finite on-resistance of HBT causes a knee voltage (V_{knee}) in the voltage waveform and it reduces voltage headroom, degrading both the output power and PAE. Those nonidealities limit the maximum efficiency to 81.9% [62].

Details of the harmonic-tuned output transformer is depicted with the aid of simplified equivalent circuits. A top view of the output transformer and a cross section of BEOL metal stacks is as shown in Figure 8 (a). The output matching up to 3rd harmonic

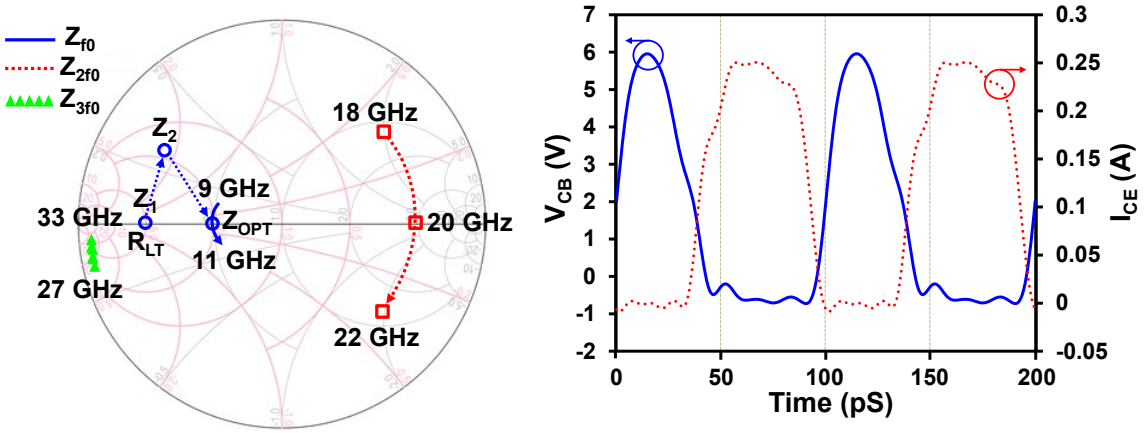


(a) (b)

Figure 8 – (a) Top view of the harmonic-tuned output transformer balun and a cross-section of BEOL and (b) an equivalent odd-mode half-circuit (lower left) and an equivalent even-mode half-circuit (lower right) of the output transformer.

frequencies are realized by exploiting primary winding inductance variation and the different impedance seen at the transformer center-tap depending on mode of operation. A transformer turn ratio was chosen to convert a 50Ω load to 25Ω for each single-ended PA unit cell. The metal line width and spacing were 20 and 3 μm, respectively, to follow by electro-migration rule. The equivalent odd-mode half-circuit of the transformer is shown in Figure 8 (b), consisting of an ideal transformer with a turn ratio of 1:(n/k), a shunt magnetizing inductance k^2L_{DM}, a series leakage inductance $(1\text{-}k^2)L_{DM}$, a parasitic capacitance C_P, and added capacitances C_1 and C_2. Multiple parameters in a blue dotted box were obtained based on EM simulation using Sonnet®. The equivalent circuit can be further simplified by shifting the load towards primary coil with proper impedance scaling, as shown in lower left of Figure 8 (b). Lower right corner of Figure 8 (b) indicates the equivalent even-mode half-circuit of the output transformer, where L_{CM} is the even-mode primary inductance and it is obtained by using following Equation 6

$$L_{CM} = \left(\frac{1 - k_P}{1 + k_P}\right) \cdot L_{DM} \tag{6}$$



(a) (b)

Figure 9 – Simulated (a) fundamental, 2nd harmonic, and 3rd harmonic impedance loci seen at the collector of the single-ended cascode cell and (b) transient waveforms of collector-base voltage (solid) and current source (dotted) for a CB HBTs in cascode.

where k_P is a self-magnetic coupling coefficient in primary winding. Simulated value of k_P is 0.25 and calculated L_{CM} is 0.26 nH at 20 GHz. To manipulate an impedance seen at collectors of CB HBTs close to open, $L_{CM} + 2L_{CT}$ must be resonated with C_P at 20 GHz. As a 2nd harmonic impedance synthesizer, a 3.4 pF dual-layered high Q MIM capacitor C_{CT} is embedded right below the center-tap of the transformer, as shown in Figure 8 (a). The C_{CT} is ac-grounded at 20 GHz, which helps to resonate C_P with $L_{CM} + 2L_{CT}$. The matching procedure and the simulated input impedance are presented on Smith chart, as shown in Figure 9 (a). The optimum impedance of 25Ω and the peak resistance of 250Ω were observed at 10 and 20 GHz, respectively. 3rd harmonic matching is also realized thanks to the combination of C_P, C_1, and self-resonant frequency nature of the output transformer.

Time domain simulation of collector-base voltage and a current for the upper HBTs in cascode are performed and plotted in Figure 9 (b). The emitter current of the CB SiGe HBTs is exploited as 1st order approximation of the CB junction current [63]. Both a half-wave rectified voltage and a quasi-square current waveform proves that the proposed harmonic-tuned output transformer supports inverse class-F mode successfully. Moreover,

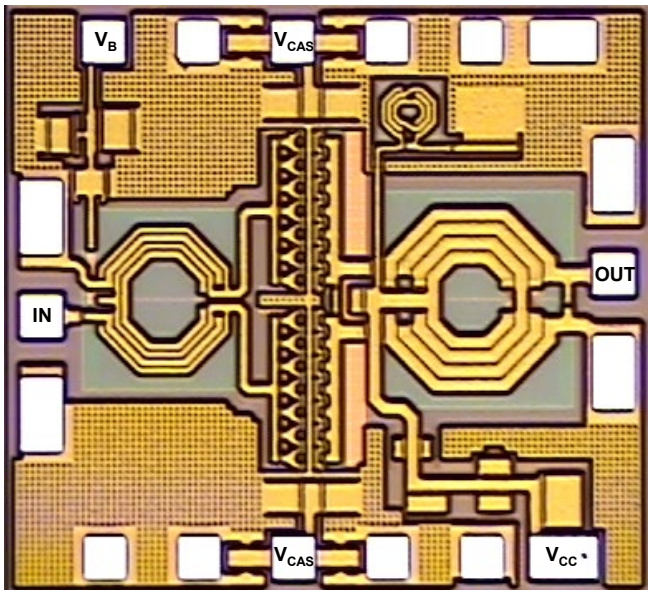
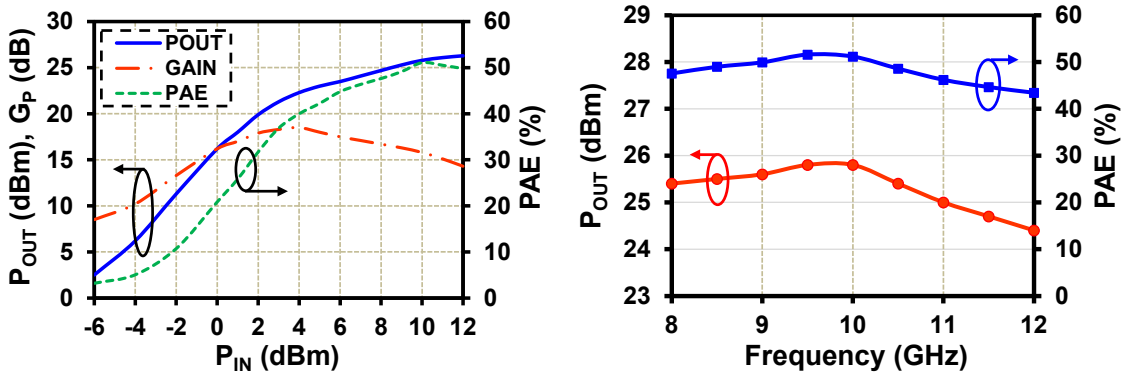


Figure 10 – Chip photograph of the first type X-band inverse-class F PA.



(a) (b)

Figure 11 – (a) Measured P_{OUT}, PAE, G_P with the input power sweep at 10 GHz, and (b) measured P_{OUT} and corresponding PAE over X-band.

the minimum overlapping of the voltage-current waveforms would extend the V_{CE} swing above BV_{CBO}, leading to increase in the output power and PAE.

The PA is fabricated in the GlobalFoundries IBM 0.12-μm SiGe BiCMOS-8HP technology with peak f_{max}/f_T of 280/220 GHz. The breakdown voltages of BV_{CBO} and BV_{CEO} are 6.0 and 1.8 V, respectively. The chip photograph is shown in Figure 10 and the

die size is 0.95 mm^2 including bond pads. The PA was characterized on wafer with 3.0 V supply. Base bias of CE and CB HBTs are 0.75 and 1.5 V, respectively, with a quiescent current of 5.2 mA. The output power, PAE, and power gain at 10 GHz were measured and plotted in Figure 11 (a). The peak PAE is 51.1% with 25.8 dBm output power and 15.8 dB power gain. The saturation power is 26.3 dBm. Next, the measured output power and PAE over X-band at the input power of 10 dBm are depicted in Figure 11 (b). The output power higher than 24.8 dBm and the PAE better than 44.6% from 8.0 to 11.5 GHz indicates a fractional 1 dB power gain bandwidth of 35%. Reliability was checked for 24 hours and it is confirmed that the proposed PA is robust to high voltage swing.

2.2 Highly Efficient X-band SiGe HBT Cascode Inverse Class-F PA With A Harmonic-Tuned Lumped-Element Wilkinson Power Combiner

Another type of sub-Watt level, highly efficient X-band SiGe HBT cascode inverse class-F PA is realized with a lumped-element harmonic-tuned Wilkinson power combiner (WPC). Compared with the transformer balun, different approach is required for WPC to support inverse class-F mode since it works in common mode at both fundamental and 2nd harmonic frequencies, which makes it difficult to do separate matching achieved in the previous design. To address this issue, a novel multi-harmonic resonance filter is designed and it is naturally merged into the lumped-element WPC to obtain required fundamental and harmonic impedance terminations for quasi inverse class-F mode. Figure 12 (a) describes a circuit schematic of the presented X-band PA. A Wilkinson power divider with an L-section matching network and a WPC with the multi-harmonic resonance filter are allocated as input and output matching network, respectively. The structure of the power cell is totally identical (the number of HBTs and the emitter area) to that of the 1st type PA.

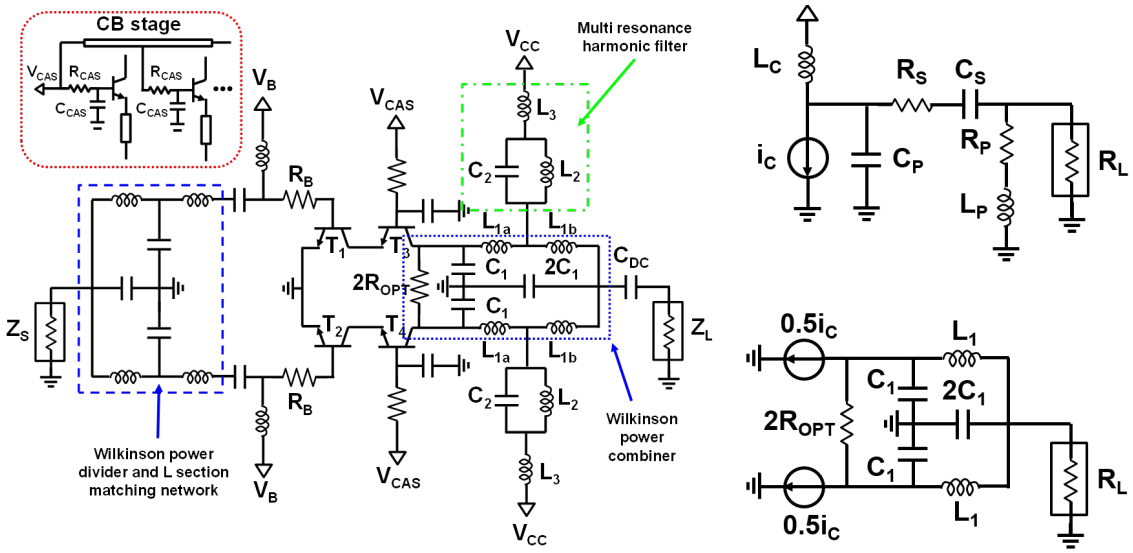


Figure 12 – Circuit schematic of (a) 2nd type X-band SiGe HBT cascode inverse-class F PA and (b) schematic of a L-section matching network (top) and schematic of a two-way lumped-element Wilkinson power combiner (bottom).

Also, layout strategy of the SiGe BHT cascode power cell is investigated in detail and it is shown in Figure 13. A single base/emitter/collector contact stripe (CBE) SiGe HBT is chosen for both CE and CB devices to simplify signal routing between them and minimize emitter inductive degeneration. When the PA is working under inverse class-F mode, voltage peaking due to 2nd harmonic impedance termination easily falls CB HBTs into impaction ionization. Thus, a very low base impedance termination is necessary to bypass avalanche generated holes without degrading power gain or causing catastrophic damage in the collector-base junction of CB SiGe HBTs. From base stripe contact to the bypass capacitor C_{CAS}, both a parasitic inductance and resistance will influence the performance and reliability of the PA. The parasitic inductance must be minimized since it would cause oscillation due to the negative input impedance seen at the emitter of the CB HBT. The parasitic resistance has two detrimental effects; one of which is lowering power

gain and another is pinch-in effect [64]. The finite resistance on base stripe of SiGe HBT and base current reversal effect induce potential gradient on the stripe, which eventually results in current hogging at the center of the base stripe. This current concentration increases the junction temperature, eventually leading to thermal runaway. To minimize both parasitic inductance and resistance, multi-layered metal stack (M1-M2-M3-M4-MQ) is used to connect between the base stripe of the CB HBTs and their corresponding dual-layered high Q MIM capacitors. With this superior BEOL, the possibility of permanent damage in SiGe HBTs can be alleviated even under large voltage swing operation.

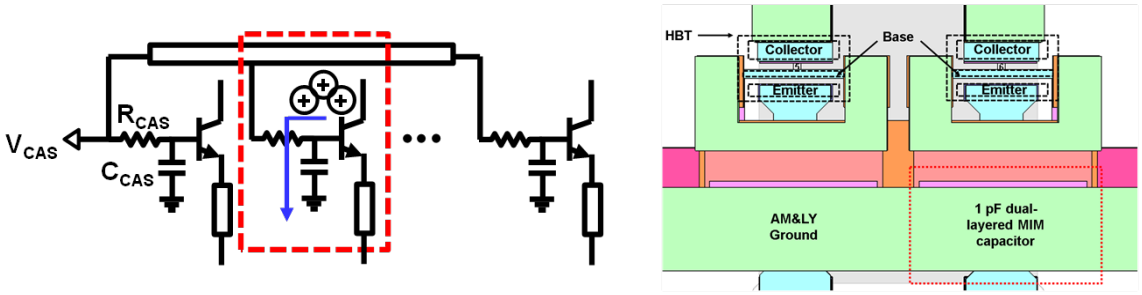


Figure 13 – Detailed circuit schematic of the CB HBTs in cascode (left) and their corresponding layout (right).

Next, design and analysis of the harmonic-tuned WPC are investigated. Figure 12 (b) depicts a circuit schematic of a single L-section matching network and a two-way lumped-element WPC, respectively. If we ignore loss of any capacitors (it is reasonable since Q-factor of capacitors is much higher than that of inductors), the passive efficiency of the two matching networks can be derived with Equation 7 below

$$\eta_L = \left(\frac{R_L}{R_L + \frac{\omega L_S}{Q_{ind}}}\right)^2 \cdot \left(\frac{Q_{ind}}{Q_{ind} + \sqrt{\frac{R_L}{R_{OPT}} - 1}}\right)^2, \quad \eta_{wpc} = \frac{Q_{ind}}{Q_{ind} + \sqrt{\frac{NR_L}{R_{OPT}}} + \sqrt{\frac{R_{OPT}}{NR_L}}} \qquad (7)$$

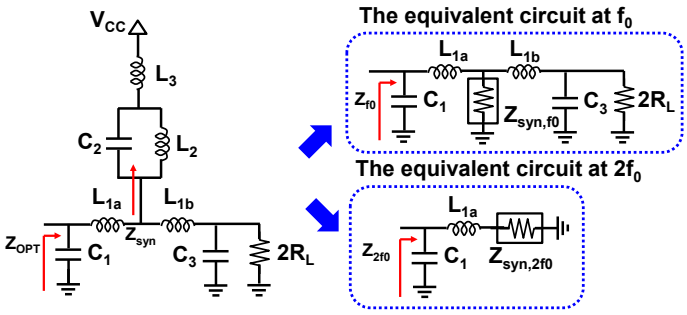
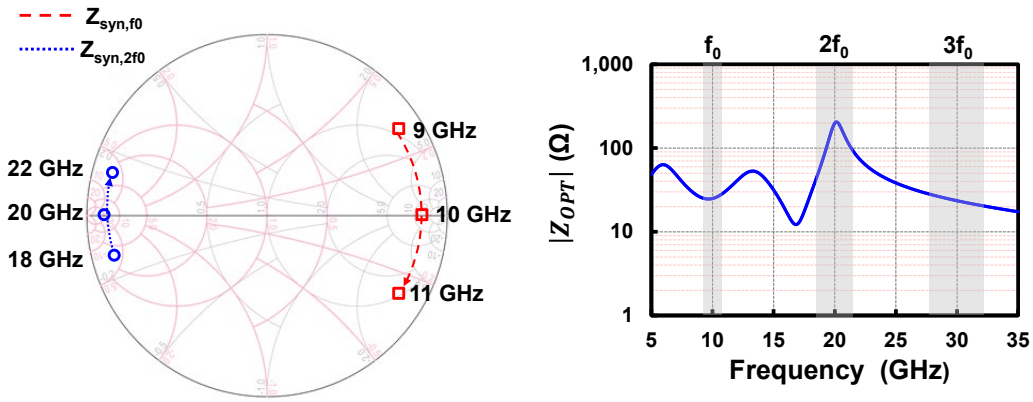


Figure 14 – Even mode half-circuit of the WPC at fundamental (top) and 2nd harmonic (bottom) frequencies and (b) simulated Z_{OPT} magnitude of the even mode half-circuit of the WPC.

where R_L is 50Ω load impedance, R_{OPT} is the optimum impedance of a transistor, Q_{ind} is the quality factor of an on-chip inductor, and N is the number of branches in WPC. If target R_{OPT} of 12.5Ω and it is assumed that C_P is resonated with L_C, calculated C_S and L_S in the single L-section matching network are 550 fF and 345 pH, respectively. On the other hands, the required C_1 and L_1 for the WPC are obtained based on following Equation 8

$$C_1 = \frac{1}{2\pi f Z_T} \quad , \quad L_1 = \frac{Z_T}{2\pi f} \tag{8}$$

where Z_T is the characteristic impedance of a λ/4 impedance transformer. It must be 50Ω to transform an even mode 100Ω load to a 25Ω R_{OPT} for each single-ended cascode cell. Calculated C_1 and L_1 are 318 fF and 796 pH at 10 GHz, respectively. If we set Q_{ind} as 20, which is reasonable value at X-band, then calculated passive efficiency of the single L-section matching network and the WPC are 81.1% and 88.9%. Figure 14 shows the even mode half-circuit of the WPC and its equivalent circuit at fundamental (top) and 2nd harmonic (bottom) frequencies. A capacitance of C_3, realized by single layer high Q MIM, is shunted to ground. A multi-harmonic resonance filer consists of a parallel C_2 and L_2 in series with L_3 and it is inserted between L_{1a} and L_{1b}. The main idea is to synthesize the



(a) (b)

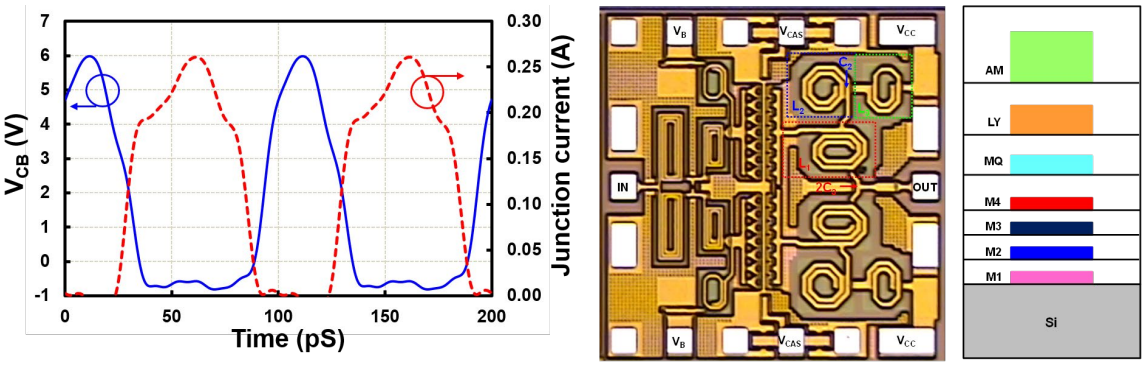
Figure 15 – (a) simulated fundamental and 2nd harmonic impedance loci (Z_{syn}) of the multi-harmonic resonance filter and (b) simulated Z_{OPT} magnitude of the even mode half-circuit of the WPC.

input impedance (Z_{syn}) of the multi-harmonic resonance filter as open and short at fundamental and 2nd harmonic frequencies, respectively. Simulated Z_{syn} is presented on a Smith chart, as shown in Figure 15 (a). The impedance of the multi-harmonic filter at 10 and 20 GHz are about 580Ω and 2.5Ω, respectively. The high impedance at the fundamental frequency hardly affects the impedance transformation of the WPC, while very low impedance at 2nd harmonic enables C_1 to resonate with L_{1a}. A capacitance C_1, which is the sum of a base to collector junction capacitance, the collector to substrate junction capacitance, and the parasitic capacitance of an interconnect at collectors of the CB HBTs, resonates with L_{1a} at the 2nd harmonic frequency, resulting in a high impedance. The L_{1a} can be derived based upon following Equation 9

$$L_{1a} = \frac{1}{C_1(4\pi f_0)^2} \quad , \quad R_{eq} = \frac{(\omega L_{1a})^2}{R_2} \tag{9}$$

Calculated L_{1a} is 198 pH with C_1 of 250 fF. Of course, fine optimization using load pull simulation is needed due to the parasitic inductance caused by the interconnect to the CB

SiGe HBTs. After a couple of iteration, L_{1a} was tuned to 178 pH. If a series to parallel conversion is applied to the equivalent half-circuit of the WPC at the 2nd harmonic, an equivalent parallel resistance R_{eq} is 200Ω at 20 GHz, which is very close to that obtained from EM simulations. Figure 15 (b) shows the magnitude response of Z_{OPT} up to 3rd harmonic frequencies. The impedance magnitudes at 10 and 20 GHz are 25Ω and 205Ω, respectively. The 3rd harmonic impedance also has a low impedance magnitude due to C_1 and capacitive behavior of the multi-harmonic resonance filter.



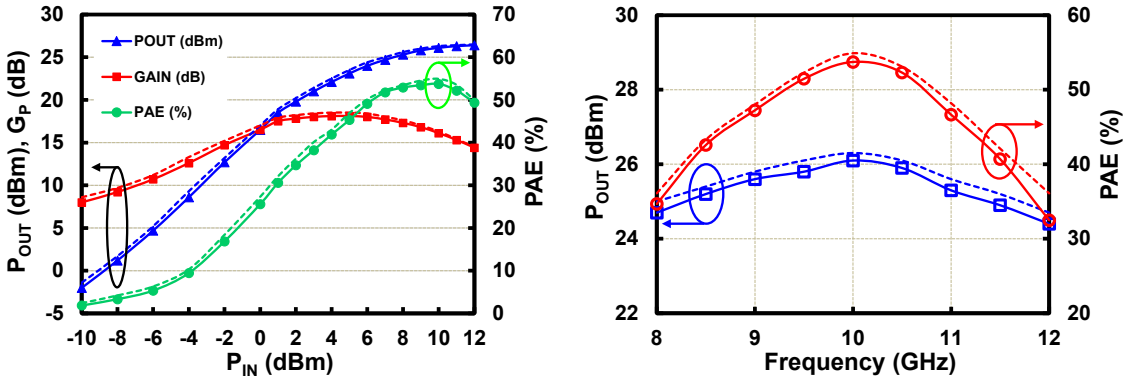
(a) (b)

Figure 16 – (a) Simulated transient waveforms of collector-base voltage (solid) and its junction current (dotted) for the CB HBTs in cascode and (b) chip photograph of the SiGe PA and a simplified cross-section of back-of-end-line (BEOL) metal stacks.

Time domain simulations of a collector-base voltage and its junction current waveform of the CB SiGe HBTs are plotted in Figure 16 (a). A quasi-square-wave current and a half-sinusoidal voltage with reduced overlap demonstrate that the proposed harmonic-tuned WPC successfully manipulates harmonic terminations for inverse class-F mode. Like the 1st type PA, the negligible junction current as the V_{CB} swings to a peak value indicates that the junction is effectively off, and thus it is protected from pinch-in effects, mitigating damage caused by avalanche multiplication and thermal runaway.

The same technology is used for implementing the PA. The chip micrograph is shown in Figure 16 (b) and it occupies 0.9 mm x 0.9 mm with bond pads. All passives, including the proposed WPC, were simulated suing the Sonnet® EM tool. The metal trace width of the harmonic-tuned WPC is 12 μm to avoid electro-migration violation. On-wafer measurement is performed and all bias setup (V_B, V_{CAS}, and V_{CC}) are identical to that of the 1st type PA design. At first, P_{OUT}, PAE, and G_P at 10 GHz with the input power sweep were plotted, as shown in Figure 17 (a). The PA delivers P_{OUT} of 26.1 dBm with 53.4% peak PAE at a 10 dBm input power, which is better than the result from the 1st type PA. The slight degradation from the simulation may stem from the inherent model mismatch of SiGe HBT and/or the EM simulations. The measured saturated output power is 26.5-dBm. The measured P_{OUT} and its corresponding PAE within X-band at the input power of 10 dBm is shown in Figure 17 (b). The 1 dB power gain bandwidth ranges from 8.6 to 11.2 GHz, with PAE higher than 42.5%, indicating a fractional bandwidth of 26%. The narrower 1 dB power gain bandwidth of the PA with the harmonic-tune WPC than that with the harmonic-tuned output transformer would be attributed to the transformer's inherent broadband characteristic. To confirm that the proposed PA withstands high voltage swing operation, P_{OUT} and collector current were monitored under CW condition. It is revealed that there is no degradation in the PA for 24-hours measurement.

Finally, state-of-the-art performance among Si-based X-band PAs is summarized in Table 1. Our works achieves the highest PAE, with either higher or comparable output power. Due to similar performance, the selection between the two PAs would depend on which input excitation is preferred in the system and DIE attachment on PCB using wire-



(a) (b)

Figure 17 – (a) Measured (symbol) and simulated (dash) P_{OUT}, G_P, and PAE with P_{IN} sweep at 10 GHz and (b) P_{OUT} and corresponding PAE over X-band at P_{IN} = 10 dBm.

bonding. Thus, those represents a potentially viable selection for highly integrated X-band phased array system implementation.

Table 1 – Comparison of State-of-The-Art Si-based X-band PAs

	[65]	[66]	[67]	[68]	[69]	[70]	**[4]**	**[58]**
Technology	180 nm SiGe	130 nm SiGe	130 nm CMOS	90 nm CMOS	180 nm CMOS	45 nm SOI CMOS	**130 nm SiGe**	**130 nm SiGe**
Class	AB	AB	AB	AB	AB	AB	**F^{-1}**	**F^{-1}**
*P_{SAT} (dBm)	26.0	29.5	23	25.0	27.1	22.5	**26.3**	**26.5**
*Peak PAE (%)	35.0	17.8	37.0	20.0	22.7	19.2	**51.1**	**53.4**
*GAIN (dB)	22.0	27.7	-	19.0	11.2	9.8	**15.8**	**16.1**
**BW (GHz)	7.2-10.2	8.0-12.0	-	6.2-11.0	7.0-10.0	9.0-15.0	**8.0-11.5**	**8.6-11.2**
Area (mm^2)	0.95	2.66	1.84	0.7***	0.88	0.22	**0.9**	**0.81**

CHAPTER 3. DESIGN OF X-BAND FRONT-END-MODULE USING SIGE HBT BICMOS TECHNOLOGY

In this chapter, the co-optimized design method of a X-band SPDT-LNA front-end-module (FEM) using SiGe HBT BiCMOS technology is proposed. At first, it is investigated in detail which design parameters are main bottlenecks in realizing the high performance, lost cost X-band FEM, and then the novel passive design scheme is devised to address the design issue. This work had been accepted in IEEE International Microwave Symposium in 2016 [71].

3.1 Co-design of a SiGe BiCMOS X-band, Asymmetric, Low Insertion Loss, High Power Handling SPDT Switch and a Ultra Low Noise LNA

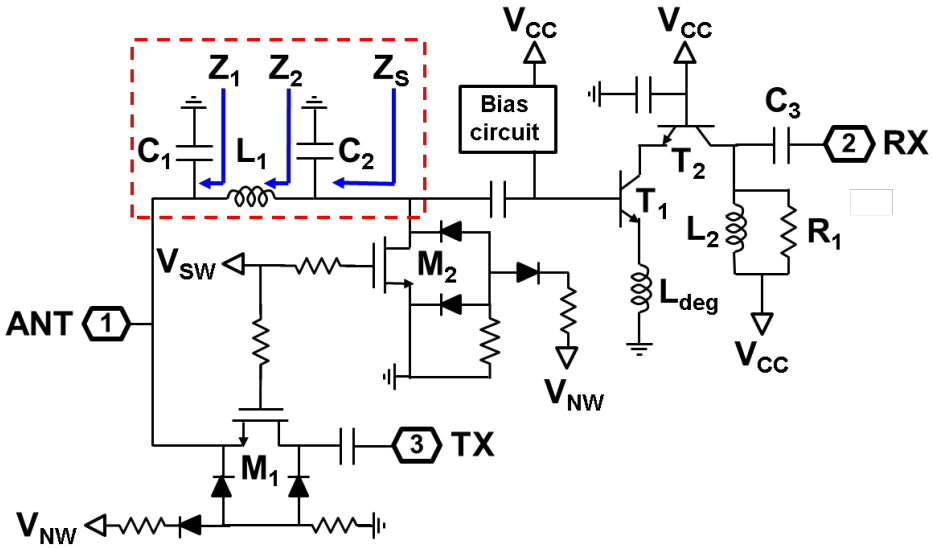


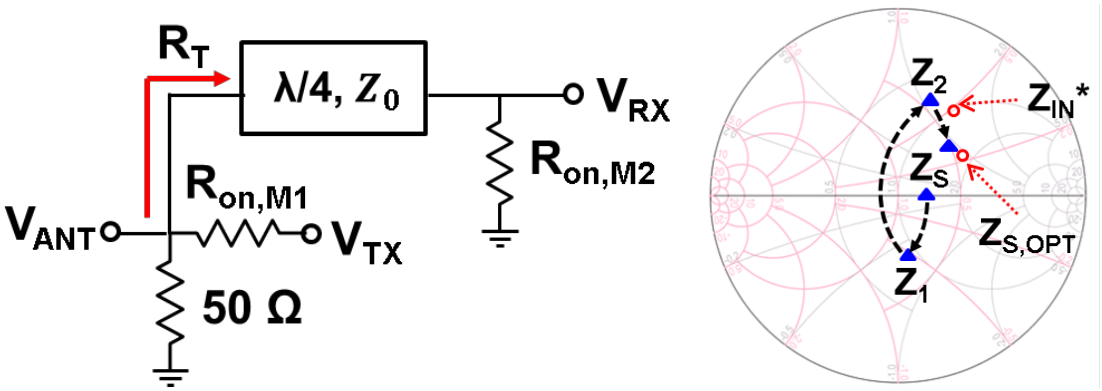
Figure 18 – Circuit schematic of the co-designed asymmetric CMOS SPDT and SiGe HBT cascode LNA.

III-V compound semiconductor technologies like GaAs and GaN have been dominated for developing high performance X-band phased arrays. However, rapid

advances in Si-based technologies with integration capability of digital signal processing makes those solutions attractive in implementing a low cost, multi-functional X-band phased array radar [72, 73] with comparable performance to their III-V counterparts. Significant research has focused on developing low cost and high performance X-band transceiver elements such as PA, LNA, and SPDT. But most of works have been solely trying to enhance each part of FEM, which would impede obtaining the best performance of insertion loss (IL), ISO, and linearity simultaneously.

In the present work, a co-optimized, asymmetric SPDT-LNA with an embedded lumped-element matching network for X-band T/R applications is developed to overcome the unavoidable trade-offs in FEM design. The circuit schematic of the proposed co-designed SPDT-LNA is depicted in Figure 18, where a red dotted box shows the embedded lumped-element matching network. The ANT port is connected to the TX port and the RX port through the SPDT. The asymmetric SPDT topology is specifically designed to handle high power in transmit mode, with less power level anticipated at the ANT and RX ports. In transmit cycle, M1 and M2 are both turned on. M1 provides a low series resistance in the transmit path and the small on-resistance of M2 is transformed through the L_1-C_1 lumped-element network to be large impedance at the ANT port. The power handling of FET switches is limited by the RF signal turning on source/drain to body junction diodes. Both FETs are turned on in the transmit state and the output power is restricted by the current handling of the series FET. In receive mode, both M1 and M2 are off. M1 provides ISO to the PA and the π-network matches the ANT port to the LNA. The ISO between the TX and ANT ports is low in receive mode, but the PA will be turned off in time division duplexing (TDD) systems and the input power at the ANT port will be low.

The FET switches is implemented with 0.13-μm triple well NMOS using the floating-body technique [33] to withstand high voltage swings. All resistor values are 10-kΩ. The size of M1 was determined by targeting an IL of 1 dB at 10 GHz. Figure 19 (a) presents the simplified equivalent circuit in transmit mode, where the on-resistance of M1 is extracted to be 5Ω to meet the IL specification. With DC I-V characteristic curve and taking parasitic capacitances of M1 into account, the total width of M1 is set to be 136 μm. In TDD system, the LNA should be turned off while transmitting power to the antenna



(a) (b)

Figure 19 – (a) equivalent lumped-element circuit in "transmit" mode and (b) Smith chart showing procedure of simultaneous input and noise matching in "receive" mode.

from the PA. If the PA delivers 0.5 W, at least 25 dB isolation is required to prevent the leakage signal from self-biasing the LNA. Theoretically calculated impedance at the ANT port looking towards the lumped-element transformer must be higher than 840Ω. The on-resistance of M2 is designed to be 4.2Ω, which is equivalent to the total width of 160 μm. Following Equation 10 is used to obtain required C_1 and L_1

$$R_T = Z_0^2/R_{on,M2} \quad , \quad Z_0 = \sqrt{L_1/C_1} = 59.4\ \Omega \tag{10}$$

the calculated C_1 and L_1 are 160 fF and 0.95 nH, respectively, with consideration of the parasitic capacitance of M1. The on-resistance of M2 is small enough that the impact of any shunt capacitance C_2 on the isolation can be negligible in transmit mode.

Cascode LNA with an inductive emitter degeneration is designed for reduced Miller effect and higher reverse isolation, which will ease the matching both at input and output. The LNA includes an internal current mirror to ensure stable biasing. The simultaneous input and noise matching is achieved through the π-network and the detailed process is plotted in Figure 19 (b). The Smith chart depicts the impedance matching from the ANT port to the base of T1 looking into source, where C_2 represents the parasitic capacitance of M2. $Z_{S,OPT}$ is the optimum noise source impedance of the LNA and Z_{IN}* is the conjugate input impedance of it. The goal is to find the optimum size of T1 such that both impedances track Z_S very closely. The geometry of T1 is chosen based on following Equation 11 [74]

$$R_{s,opt} = \frac{\omega_T}{\omega} \cdot \frac{1}{L_E} \sqrt{\frac{2r_b L_E}{J_C W_E} \cdot \frac{kT}{q}} \quad , \quad Z_{IN} = \frac{1}{j\omega C_{be}} + j\omega L_{deg} + \omega_T L_{deg} \tag{11}$$

In Equation 11, $R_{S,OPT}$ decreases as the emitter length L_E increases. Equation 11 indicates that the real part of the input impedance looking into the base of T1 increases with the emitter degeneration inductance, L_{deg}, realized by a narrow width microstrip T/L. The optimization is carried out iteratively, and as a result, T1 has an emitter length of 15 μm with 3 emitter stripes. CBEBC SiGe HBT is used for T1 and T2 to reduce the explicit base stripe resistance and thereby minimizing the impact of the base resistance on noise figure and gain. The value of L_{deg} is derived from Equation 11 and was simulated using Sonnet®,

which results in the equivalent inductance of 150 pH. For output matching, a 170Ω resistor, R1, is placed in parallel with a L2 to broaden the bandwidth and stabilize the LNA.

3.1 Measurement and Comparison

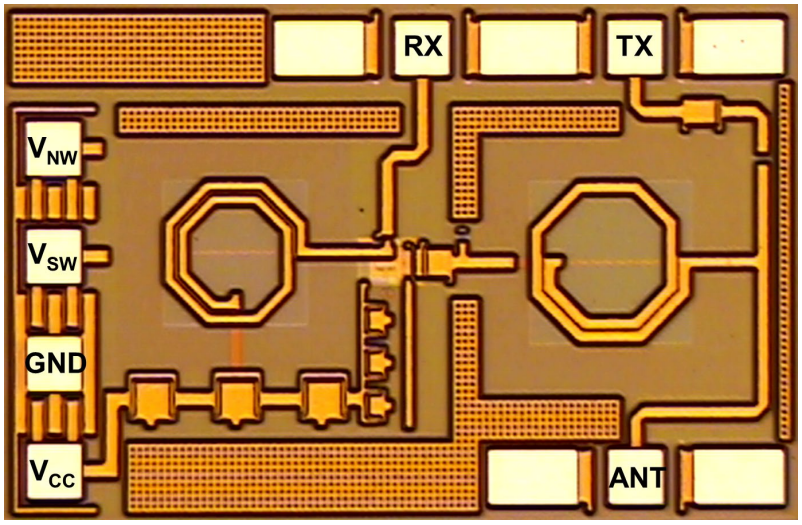


Figure 20 – Microphotograph of the asymmetric SPDT-cascode LNA.

The co-designed asymmetric SPDT-cascode LNA is implemented in the Global Foundries 0.12-μm BiCMOS-8HP technology. The chip photograph is shown in Figure 20 and it occupies a total area of 0.5 mm^2 excluding bond pads. The measurements were performed with a Keysight E8364B four-port network analyzer from 5 to 15 GHz.

A standalone SPDT was measured to derive the isolation (ISO) from the TX port to the LNA input. The M1 and M2 are turned on/off with V_{SW} = 1.4/0.0 V. The simulated and measured S-parameters of the SPDT in transmit mode is shown in Figure 21 (a). The measured insertion loss (IL) is 1.1 dB, very close to the simulation. The measured 0.5 dB IL bandwidth is from 7.2 to 15.0 GHz, wholly covering X-band. The measured IL of the SPDT-LNA, plotted as circle line in Figure 21 (a), is almost identical to that from the SPDT. The measured isolation is 26 dB at 10 GHz and higher than 24 dB from 8 to 12

GHz. The return losses (RLs) of the TX port and the ANT port are higher than 10 dB at X-band. The cascode LNA was biased to V_{CC} = 2.4 V, which consumes 21.6 mW. The simulated and measured results are shown in Figure 21 (b). The measured gain is 15 dB at 10 GHz, which is 1 dB lower than the simulated result. The discrepancy could be caused by the unavoidable mismatch between schematic and layout, which would include the imperfect ac grounding at the base of T2. The RL both at the ANT and RX ports are more than 10-dB from 9 to 11 GHz.

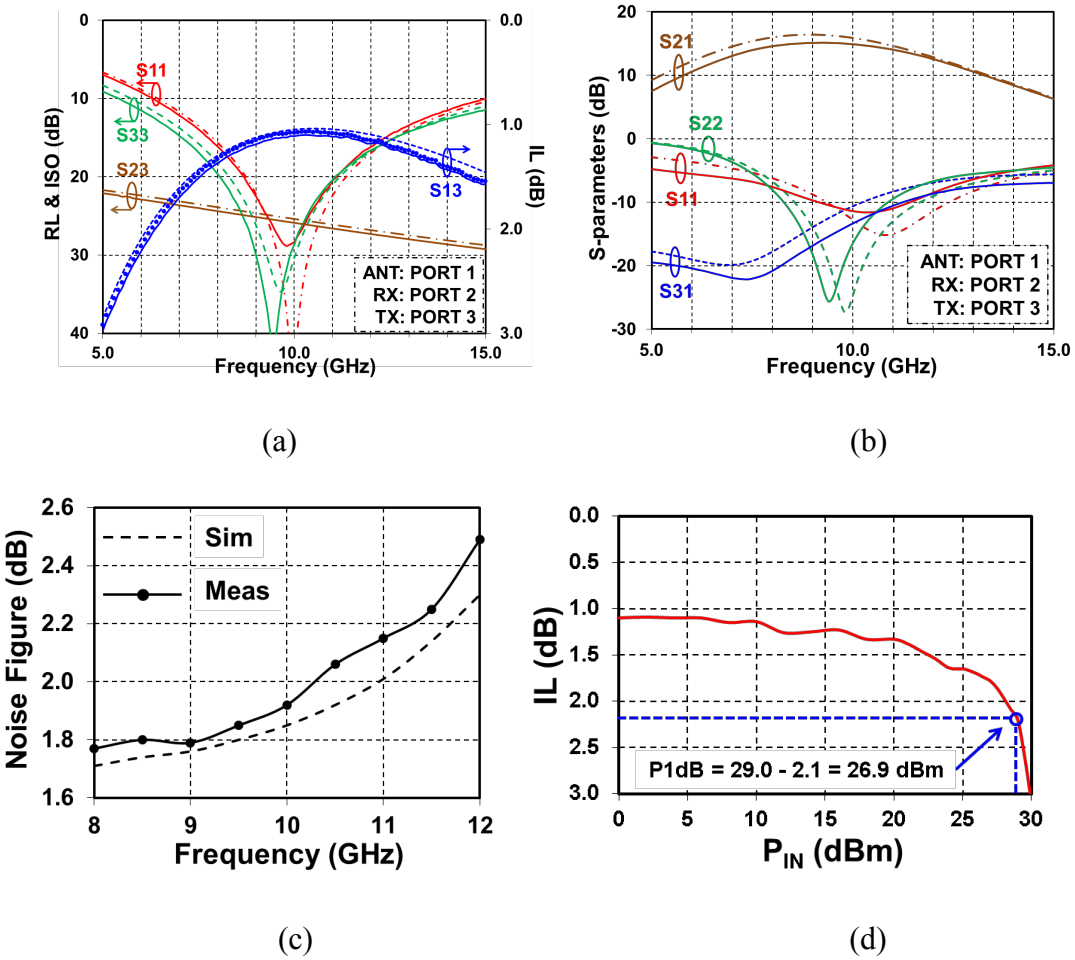


Figure 21 – (a) simulated (dashed) and measured (solid) S-parameters of the asymmetric SPDT in transmit mode (b) the asymmetric SPDT-cascode LNA in receive mode (c) Simulated (dashed) and measured (solid) noise-figure of the co-designed SPDT-LNA in receive mode and (d) measured output P1dB of the co-optimized SPDT-LNA in transmit mode.

The noise figure (NF) was measured using an Agilent N9030A spectrum analyzer and an N4002A noise source, with careful calibration to compensate for probe and cable losses. Ten samples were taken for measurement and then averaged to reduce error. Figure 21 (c) shows that the measured NF at 10 GHz is 1.9 dB, very similar with the simulated result of 1.84 dB. The NF remains below 2.2 dB up to 11.3 GHz. Finally, the power handling capability in transmit mode is measured by monitoring the output P1dB with 1-dB step. As shown in Figure 21 (d), thee measured output P1dB at 10 GHz is 26.9 dBm, which demonstrates the proposed SPDT has high linearity characteristic.

Table 2 compared state-of-the-art X-band SPDTs and LNAs. The NF estimation of a SPDT-LNA chain with the bulk Si-based works would be 2.3 dB at 10 GHz, which is still 0.4 dB higher than the presented work. The proposed circuit also proves the highest output P1dB in transmit mode for any currently reported bulk Si-based SPDTs. All results prove that the proposed lumped-element C-L-C π-network, used for the isolation in transmit mode as well as simultaneous input and noise matching for the LNA in receive mode, will be beneficial in optimizing multiple design metrics of the FEM. Therefore, the proposed asymmetric NMOS SPDT and SiGe HBT cascode LNA combo would be viable solution for high performance X-band transmit/receive modules.

Table 2 – Comparison of State-of-The-Art Si-based X-band SPDTs and LNAs

Reference	Circuit type	Technology	Gain (dB)	NF (dB)	IL/ISO (dB)	Output P1dB (dBm)	Area (mm^2)
[59]	LNA	180 nm SiGe BiCMOS	24.2	1.3	-	-	0.46
[34]	SPDT	180 nm Bulk CMOS	-	-	1.0/32.0	23.0	0.06
[75]	SPDT	250 nm SiGe BiCMOS	-	-	2.3/39.0	24.3	0.73
[76]	SPDT	45 nm SOI CMOS	-	-	0.6/17.0	30.9	0.09
[71]	**SPDT+LNA**	**130 nm SiGe BiCMOS**	**15.0**	**1.9**	**1.1/26.0**	**26.9**	**0.50**

CHAPTER 4. DESIGN OF A WIDEBAND POWER DIVIDER/COMBINER AND A BROADBAND DISTRIBUTED POWER AMPLIFIER USING SIGE HBT BICMOS PROCESS

In this chapter, the design of a wideband power combiner and a broadband SiGe HBT power amplifier are presented. In a chapter 4.1, the compact, highly efficient, and wideband lumped-element Wilkinson power divider/combiner (WPDC) is proposed to increase the output power of PAs over a broad range of frequency. This work had been accepted in IEEE Microwave and Wireless Components Letter in 2017 [77]. A chapter 4.2 introduces an extended design methodology of the WPDC with an impedance transformation capability and it is applied to a SiGe HBT cascode non-uniform distributed PA for the broadband amplification. The combination of the proposed WPDC and the distributed PA architecture using SiGe HBT BiCMOS technology would be a viable solution in implementing a variety of broadband wireless applications.

4.1 A Compact, Low loss, and Broadband Lumped-Element Wilkinson Power Divider/Combiner Using Symmetric Inductors With Embedded Capacitors

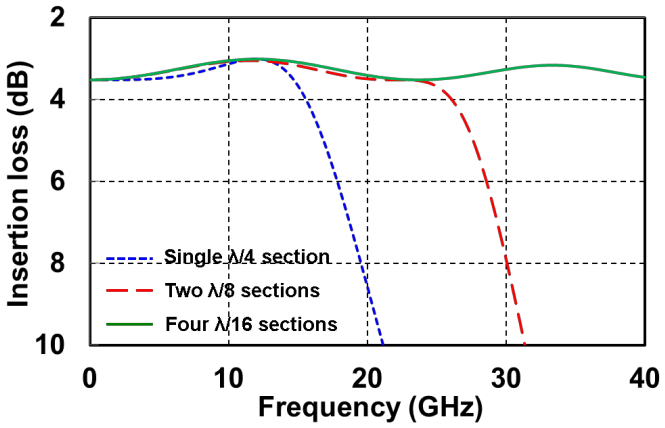


Figure 22 – Simulated insertion losses (ILs) of lumped-element WPDCs for λ/4 impedance transformers designed with the number of C-L-C pi networks variation.

Rapid advances in Si-based technologies have enabled those solutions for wideband phased array and high-resolution imaging to attain comparable performance at reduced cost compared with their III-V counterparts. Among many circuit elements in a transceiver, a high power and wideband PA would be an indispensable component. Therefore, compact and broadband power divider/combiners are getting the spotlight for combining multiple PAs to boost the output power.

Among many power combiners, Wilkinson power divider/combiner (WPDC) have been widely used for equal power distribution and combining due to its low loss, high isolation, and robustness to mismatch. Conventional WPDC, however, is not appropriate for integration because it requires at least two $\lambda/4$ transmission lines (T/Ls), and thus occupying large chip area. Thus, continuous efforts have been made in reducing foot-print while keeping its attractive features including; a lumped-element WPDC [78], a WPDC using a slow-wave T/L [79], a WPDC with capacitive loading [80], and a differential WPDC using coupled inductors [27]. Among those, the lumped-element WPDC will be the best solution for die area saving since it uses inductors and capacitors, instead of bulky T/Ls, to realize a $\lambda/4$ impedance transformer. But, the lumped-element WPDC has band-limited nature induced by the cut-off frequency of a LC π-network, which necessitates dividing the single LC section into multiple LC sections. Figure 22 is simulated insertion losses (ILs) of lumped-element WPDCs for various $\lambda/4$ impedance transformers designed with different number of LC sections. Ideal inductors and capacitors are exploited for the simulation. The results clearly show the bandwidth extension with the increase in the number of LC π-networks, but this also means more required inductors, which would increase IL and consume more Si area.

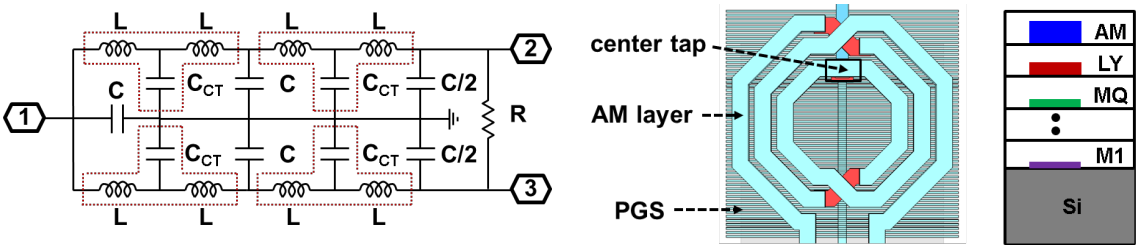


Figure 23 – Circuit schematic of the proposed wideband lumped-element WPDC (left) and a top view layout of a symmetric inductor with an embedded capacitor at its center tap (right).

To resolve this issue while leveraging it as an advantage, we proposed a compact, highly efficient, and broadband lumped-element WPDC. Figure 23 shows a circuit schematic of the devised WPDC and a top view layout of a symmetric inductor exploited in realizing an artificial λ/4 impedance transformer. Each impedance transformer consists of four-section LC π-networks to reduce the impact of the cut-off frequency on its bandwidth. A red dotted box indicates a patterned ground shield (PGS) symmetric inductor with a capacitor C_{CT} embedded at its center tap, which is equivalent to the cascade of two λ/16 LC π-networks. This simple but novel layout technique decreases the number of required inductors by half compared with a conventional LC π-network, and helps maintain symmetry, making it robust to process variation. Two series-connected symmetric inductors in each arm of the proposed lumped-element WPDC form the cascade of four λ/16 LC π-networks for the λ/4 impedance transformer, resulting in size reduction and bandwidth extension simultaneously. The values of L and C were determined based on following Equation 12 and Equation 13

$$T_D = \frac{\varphi}{2\pi f} = n\sqrt{LC} \quad , \quad Z_T = \sqrt{L/C} \tag{12}$$

$$C = \frac{T_D}{nZ_T} \quad , \quad L = CZ_T{}^2 \tag{13}$$

where T_D is the delay of a LC π-network, n is the number of LC π-networks, and Z_T is the characteristic impedance of λ/4 impedance transformers. Theoretical values of L and C are 368 pH and 74 fF at 12 GHz, respectively. By taking parasitic capacitance of the symmetric inductors into account, the actual values of L and C were tuned to 371 pH and 51 fF, respectively. The combination of a 4 μm thick aluminum top metal layer (AM) and PGS (M1) underneath an inductor enables the symmetric inductor realization with the quality factor of 20 at 12 GHz. The trace width and spacing between adjacent turns of the symmetric inductor are 8 μm and 3 μm, respectively. All capacitors in the schematic are single-layered high Q MIM capacitor sandwiched between AM layer and LY layer. C_{CT}, ideally equal to C, was shunted to ground through MQ layer and it is tuned to 49 fF. Two MIM capacitors in series are used to realize C/2 at ports 2 and 3. The isolation resistor R of 100Ω is realized with a BEOL resistor, located just above MQ layer. Unlike poly or diffusion resistors, the BEOL resistor is far removed from lossy Si substrate, and isolation degradation coming from interconnect parasitic can be minimized. The layout was made fully symmetric to minimize both amplitude error and phase mismatch between port 2 and port 3. The whole structure was EM-simulated through Sonnet® tool.

The proposed compact, low loss, and wideband WPDC was implemented in the GlobalFoundries IBM 0.12-μm SiGe BiCMOS-8HP technology. The chip microphotograph is depicted in Figure 24 and the core chip size is 0.32 x 0.34 mm^2. The measurement with a Short-Open-Load-Thru (SOLT) calibration was performed by using a Keysight E8364B four-port network analyzer, from DC to 20 GHz. Probe pads and interconnects of the WPDC are de-embedded with "pad-open-short" structures [81], to accurately compensate for the loss of them.

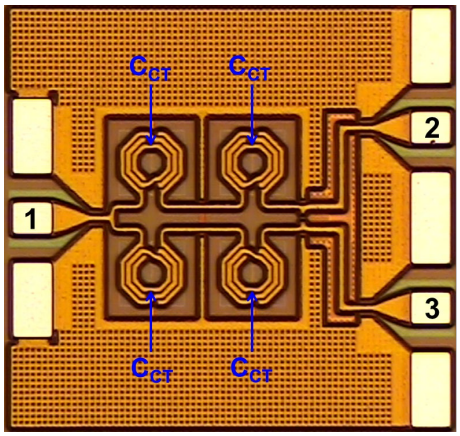


Figure 24 – Chip photograph of the fabricated lumped-element WPDC.

Figure 25 (a) and (b) compares simulated and measured S-parameters of the proposed WPDC. The excellent matching between the simulation and the measurement is observed. The minimum insertion loss (IL) of 0.45 dB at 10 GHz is equivalent to a passive efficiency of 90.1%. IL less than 1 dB, isolation (ISO) better than 10 dB, and return loss (RL) higher than 10 dB are all satisfied from 5.2 to 18.8 GHz, and thus the proposed WPDC covers C-, X-, and Ku-band seamlessly. The IL is a little degraded at high frequency corner and it may stem from unaccounted parasitic capacitance at port 1, which coincides with the frequency downshift in S11. Amplitude mismatch and phase error between the paths from port 1 to port 2 and to port 3 are plotted in Figure 25 (c). The measured imbalance in the amplitude and the phase are less than 0.06 dB and 1.0° from DC to 20 GHz, respectively, which proves that the proposed lumped-element WPDC is insensitive to process variation.

At last, the performance of state-of-the-art WPDCs is summarized on Table 3. The present work has the lowest IL and the most broadband characteristic, with similar or smaller chip area consumption. Thus, the proposed compact, highly efficient, and wideband lumped-element WPDC using symmetric inductors with embedded capacitors at their center-tap would be a promising solution for broadband power combining.

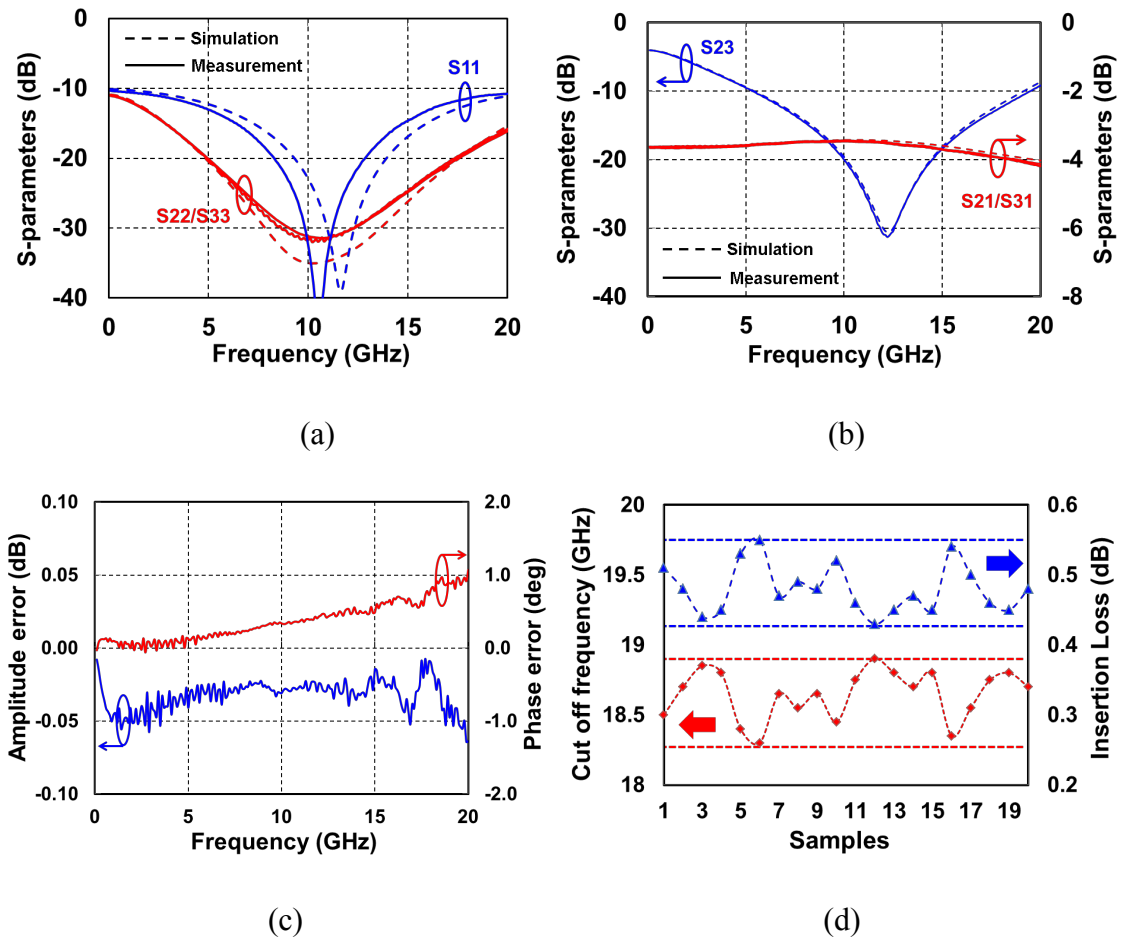


Figure 25 – Simulated (dashed) and measured (solid) S-parameters of (a) RLs (b) ILs/ISOs (c) measured amplitude and phase errors between the two arms in WPDC and (d) the bandwidth (red) and IL (blue) variation over 20 chips.

Table 3 – Comparison of Wilkinson Power Divider/Combiners

	[78]	[28]	[27]	**[77]**
Tech.	High resistivity Si	High resistivity Si	0.35 μm SiGe BiCMOS	**0.13 μm SiGe BiCMOS**
Topology	Lumped-element	Capacitive loading	Lumped-element	**Lumped-element**
*Freq. (GHz)	5.5 ~ 11.5	N/A	8.0 ~ 14.0	**5.2 ~ 19.5**
*BW (%)	71	**45	54	**116**
IL (dB)	0.6 @ 8.5 GHz	0.55 @ 10 GHz	1.25 @ 10 GHz	**0.45 @ 10 GHz**
ISO (dB)	12.8 @ 8.5 GHz	> 15 @ 10 GHz	15 @ 12 GHz	**30 @ 12 GHz**
***Amp. error (dB)	N/A	N/A	< 0.6	**< 0.06**
***Phase error (°)	N/A	N/A	< 3.0	**< 1.0**
Area (mm^2)	0.12	1.3	0.12	**0.11**

*Freq. and BW is defined as the frequency range satisfying the following conditions: ISO > 10.0 dB and RL > 10.0 dB.

** It is obtained only based on RL.

4.2 A 2-19 GHz SiGe HBT Cascode Non-Uniform Distributed Power Amplifier Using Lumped-Element Two-section λ/4 Transformer-Based Wilkinson Power Divider/Combiner

Signal amplification over ultra-wideband is becoming crucial for a variety of applications, such as software reconfigurable radios, high-speed data links, high-resolution pulse-based imaging, electronic warfare, space technology, and high-end test equipment. A power amplifier would be the most critical component in a system because high output power generation over more than one octave bandwidth is extremely challenging task. Among many design techniques, a distributed amplifier topology will be the most popular choice for its inherent broadband characteristic, which is obtained by absorbing parasitic capacitances of transistors into input and output transmission lines [82].

III-V compound processes, especially GaN technology, have dominated the development of Watt-level distributed power amplifiers (DPAs) due to its high breakdown voltage and superior speed [83]. To lower their cost and increase integration level advantages, vigorous studies have been carried out to develop high power Si-based DPAs. Stacking transistors [84-86], used a as power cell in a DPA, are being highlighted as one viable design methodology, since it enables to increase supply voltage without device breakdown and helps obtain optimum impedance close to 50Ω for wideband operation. Phase misalignment of voltage swing at the drain/collector of transistors and a very small bypass capacitor at the gate/base of each stacked transistor, however, limit the number of transistor stacking to either 3 or 4. As a result, the output power (P_{OUT}) of reported CMOS and SiGe HBT stacked DPAs are still in the range of 20 dBm, insufficient for implementing Watt-level broadband DPAs. A uniform two-stacked SiGe HBT DPA [87] with lumped-

element transmission lines (T/Ls) also demonstrated P_{OUT} of 20 dBm, but its narrow bandwidth would be attributed to a very high characteristic impedance of the output T/L in the first stage. To resolve this issue, the non-uniform DPA (NDPA) with unequal transistor geometry [88] was presented. But the characteristic impedance of microstrip T/Ls realized in the back-end-of-line (BEOL) of Si-based technologies is usually less than 70Ω due to the limited current handling, which eventually impedes adopting the NDPA topology to multi-stage Si-based DPAs. This limitation is easily explained with the aid of Equation 14, obtained from [89]

$$Z_{o,n} = \frac{R_{opt} R_L}{R_{opt} - R_L \sum_{i=n+1}^{N} L_{E_i}} \tag{14}$$

where $Z_{o,n}$ represents a characteristic impedance of *nth* output T/L, R_{opt} is the normalized optimum impedance (the unit is Ω·μm), R_L is a load resistance (it is usually 50Ω), and L_{Ei} is the total emitter length of *ith* power cell in a NDPA. From the Equation 14, lowering the load resistance is a key toward improved performance of NDPAs. The reduced load resistance in the NDPA will decrease required characteristic impedance of output T/Ls, which makes those T/Ls more realizable and tolerable at high current operation. It also provides a chance to widen the total emitter area of SiGe HBTs in the distributed PA for obtaining higher output power. This improvement only holds if an output impedance transformation network supports the wideband operation.

To address these challenges, we proposed a sub-Watt level SiGe HBT cascode NDPA. A symmetric inductor with an embedded capacitor at its center-tap [77] is used to design lumped-element base and collector T/Ls in the NDPA to alleviate the impact of the

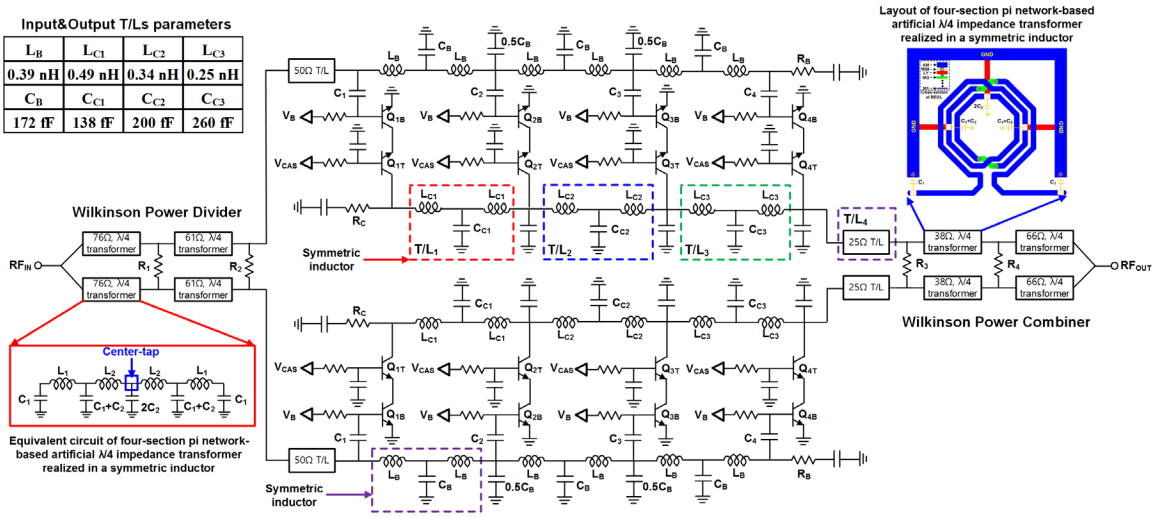
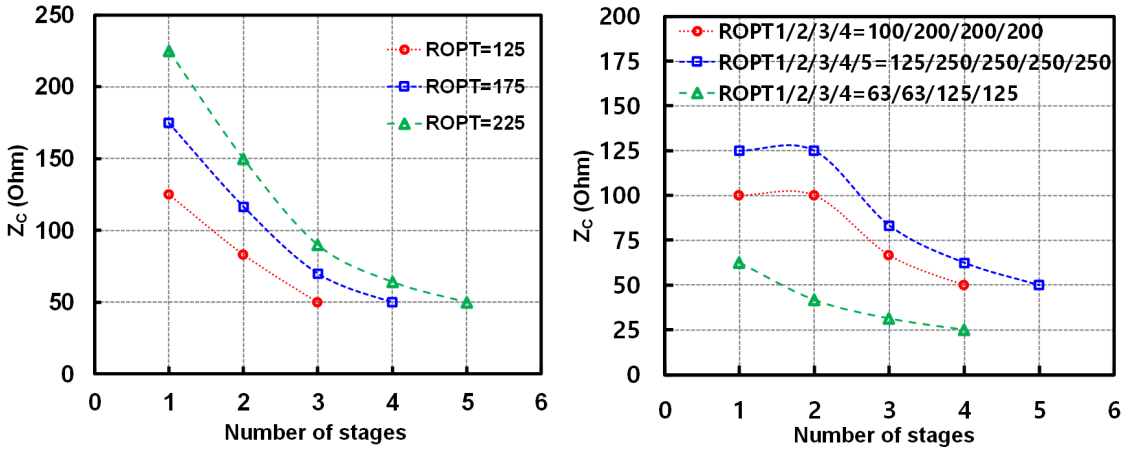


Figure 26 – Circuit schematic of the proposed NDPA with lumped-element WPDC. Dotted box in the DPA core shows both input and output T/Ls and upper right corner table summarized design parameters of the input and output T/Ls.

cut-off frequency of a pi network on the bandwidth reduction. A compact and wideband lumped-element two-section λ/4 transformers-based Wilkinson power divider and combiner (WPDC) is proposed for further increasing P_{OUT}. An artificial λ/4 impedance transformer in the WPDC is designed by cascading four C-L-C pi networks integrated into a single 3-turn symmetric inductor, which dramatically saves Si area and achieves high passive efficiency. In addition, the Wilkinson power combiner transforms an output load from 50 to 25Ω, which helps to reduce the required characteristic impedance of collector T/Ls. As a result, an increment in the number of stages and/or widening SiGe HBT emitter area are possible for high gain and P_{OUT}. The proposed NDPA delivers the peak P_{SAT} of 24.2 dBm with 3 dB bandwidth from 2 to 19 GHz, which is the highest output power with comparable operating bandwidth in any Si-based DPAs reported to date.

Figure 26 describes a circuit schematic of the proposed NDPA. It consists of a two-section lumped-element Wilkinson power divider, two 4-stage SiGe HBT cascode DPA parallel cores, and a two-section lumped-element Wilkinson power combiner. At first,



(a) (b)

Figure 27 – Characteristic impedance of collector T/Ls for (a) uniform DPA with 50Ω load and (b) non-uniform DPA (NDPA) with 50 and 25Ω load.

the non-uniform design technique with a lower load impedance is adopted for the DPA to reduce the characteristic impedance of collector T/Ls, which enables to increase the number of stages and/or the emitter area of SiGe HBTs, leading to higher P_{OUT} and gain, with wide bandwidth. As summarized in a table in Figure 26, both input and output T/Ls were realized by a symmetric inductor with a MIM capacitor at its center tap, which have the cutoff frequencies about two times higher than those of a single C-L-C pi network-based T/Ls and helps to maintain the wide bandwidth of the NDPA. The characteristic impedance of collector T/Ls were determined by Equation 15 and Equation 16 [83]

$$G_1 = G_C = G_{OPT,1} \tag{15}$$

$$G_i = \frac{{G_1}^2}{G_C + G_1} + \sum_{k=2}^{i} G_{OPT,k} \text{ where } i = 2,3,4,\ldots \tag{16}$$

where $G_{OPT,i}$ is the optimum conductance of *ith* cascode power cell, G_i is the characteristic conductance of *ith* output T/L, and G_C is a dumping conductance at the output. Figure 27

(a) and (b) show required characteristic impedance (Z_C) of collector T/Ls for a uniform DPA and a non-uniform DPA (NDPA), respectively. With a fixed load of 50Ω, the uniform DPA has limitation on the maximum number of stages with relatively low Z_C or very high Z_C is required to increase the number of stages. For example, Z_C of 225Ω for the first collector T/L is necessary for the 5-stage design. If the load impedance is lower than 50Ω, the required Z_C at collector T/Ls will be relaxed and reduced. Those more realizable characteristic impedance of the output T/Ls in the NDPA decrease the absolute value of a required inductance in a lumped-element T/L, which results in Q factor increase and higher self-resonant frequency. Thus, it is reasonable to assert that the NDPA core with the lower load has wider bandwidth than that with 50Ω load if an output impedance transformer is able to maintain the bandwidth of the NDPA core.

If a peak-to-peak voltage swing of a SiGe HBT cascode is assumed to be 4.6 V_{PP}, a theoretical total emitter area of the DPA for 26 dBm generation (by ignoring an output matching network loss) is 33 μm^2. Based on the estimated value, the emitter area of each cascode power cell in the single NDPA core are 5.76, 5.76, 2.88, and 2.88 μm^2 from the first stage to the last stage, which corresponds to $R_{OPT1/2}$ of 63Ω and $R_{OPT3/4}$ of 125Ω. Inserting the optimum impedance values into Equation 15 and Equation 16 leads the characteristic impedances of the output T/L_1, T/L_2, T/L_3, and T/L_4 to 63Ω, 42Ω, 31.5Ω, and 25Ω, respectively. The line widths of symmetric inductors at the collector of the NDPA core get wider from a stage to its subsequent stage to avoid violating electromigration rules at high current operation. At input side, 50Ω lumped-element T/Ls are phase-synchronized with their corresponding output T/Ls and the input T/Ls are identical for simplifying the design. Dumping resistors R_B (50Ω) and R_C (63Ω) guarantee flat gain and good

input/output return losses over the wide bandwidth by absorbing waves traveling in the reverse direction. A low impedance termination at the base of upper SiGe HBTs (Q_{iT}) and a series capacitive coupling (C_i) at the base of lower HBTs (Q_{iB}) in cascode increases the voltage excursion for higher P_{OUT} and decreases the effective capacitance at the base for bandwidth extension, respectively. Dual MIM capacitor array layout technique [56] is adopted to the base of upper SiGe HBTs in cascode, which minimizes the parasitic inductance and stabilize the PA. The series capacitance of $C_{1/2}$ and $C_{3/4}$ are set to 100 and 150 fF, respectively, for the 50Ω input lumped-element T/Ls. Shunt capacitors to ground are added on the output of 2nd, 3rd, and the last cascode power cells for the phase alignment between the input and output T/Ls. The Wilkinson power divider transforms a common 100Ω source to a 50Ω input impedance of each NDPA and the Wilkinson power combiner lowers a common 100Ω load to a 25Ω optimum impedance for a single NDPA core. Termination resistors of R_1, R_2, R_3, and R_4 in the WPDC are 94Ω, 207Ω, 123Ω, 67Ω, respectively, determined by [90]. Bias resistors decouple a RF signal from a DC supply.

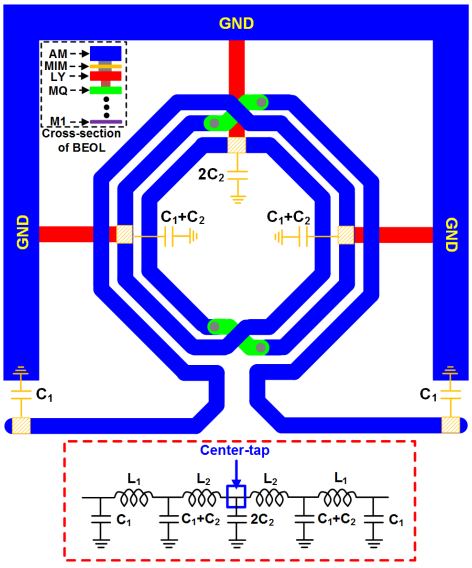


Figure 28 – Top view of a lumped-element λ/4 impedance transformer realized in a single symmetric inductor (top) and its corresponding equivalent circuit (bottom).

Next, the details of two-section lumped-element λ/4 transformer-based WPDC design are illustrated. For widening bandwidth, the number of series λ/4 impedance transformers in each arm of WPDC should be increased, but it also entails increasing chip area and passive efficiency degradation [91]. A lumped-element artificial λ/4 impedance transformer is frequently used for Si area reduction but its bandwidth is severely limited by the cutoff frequency of a C-L-C pi network. [77] proposed a multi-section pi networks scheme for bandwidth expansion, but it still requires two series inductors for a single λ/4 impedance transformer synthesis.

To resolve the bandwidth limitation while obtaining compact size, a novel four-section pi network-based lumped-element λ/4 transformer is designed. At first, characteristic impedance of lumped-element λ/4 transformers in WPDC is determined based on Chebyshev design coefficients [92] to maximize the bandwidth. Figure 28 is a top view layout of a lumped-element λ/4 transformer in the WPDC. The main idea is to divide the inductor into four-sections, each symmetrical with respect to its center-tap, by locating MIM capacitors at proper places, as highlighted in the figure. As a result, two pi networks (C_1-L_1-C_1 and C_2-L_2-C_2) with a very high cutoff frequency form an artificial λ/4 transformer very close to ideal value of unity. Metal dummy fill cells, from M1 to AM layers, are used as the ground termination of the MIM capacitors. An important design issue is how to estimate the ratio between L_1 and L_2 in the symmetric inductor. It was discovered through EM simulations while using the multiport inductors extraction method [93] that any 3-turn symmetric inductor has L_1:L_2 ratio ranging from 3:2 to 6:5 depending on its size. Once the ratio is known, it is easy to obtain capacitances C_1 and C_2 for a specific characteristic impedance based on the image parameter method [92]

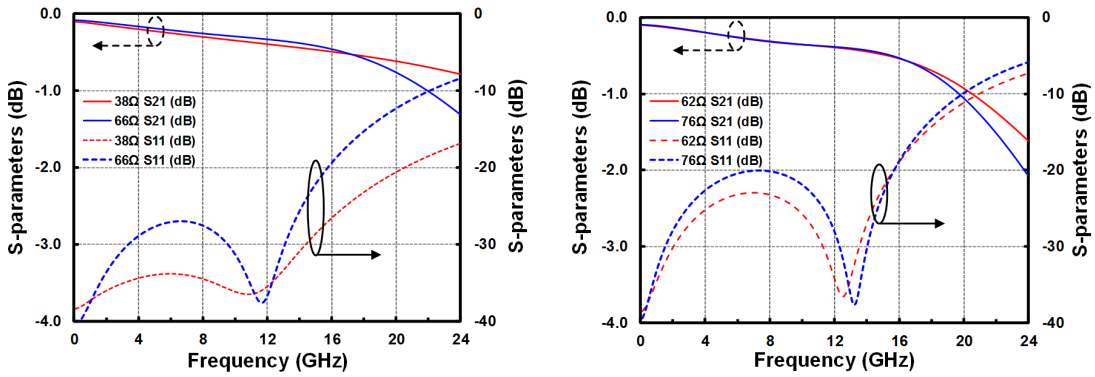
$$Z_0 = \sqrt{\frac{L}{C}} \quad , \quad f_c = \frac{1}{\pi\sqrt{LC}} \quad , \quad Z_{i\pi} = \frac{Z_0}{\sqrt{1-(\frac{f}{f_c})^2}} \tag{17}$$

$$\phi = \frac{180}{\pi} \cdot \mathrm{imag}\left[\ln\left(1 - 2\left(\frac{f}{f_c}\right)^2 + 2\frac{f}{f_c}\sqrt{\left(\frac{f}{f_c}\right)^2 - 1}\right)\right] \tag{18}$$

where Z_0 is a nominal characteristic impedance, f_c is a cutoff frequency of the pi network, $Z_{i\pi}$ is an image impedance of the pi network, and ϕ is a phase of the pi network. With the turn ratio L_1:L_2 of 3:2, the numerical iterations of Equation 17 and Equation 18 are converged to L_1/L_2 and C_1/C_2 of 230/154 pH and 84/55 fF at 12 GHz, respectively, for the 38Ω λ/4 transformer. The EM result leads to the optimum diameter of 112 μm for the symmetric inductor. Due to parasitic capacitance of each inductor segment, capacitances C_1, $C_1 + C_2$, and $2C_2$ are tuned to 75 fF, 130 fF, and 96 fF for the 38Ω lumped-element λ/4 transformer, respectively. Identical design procedure was taken to implement other λ/4 impedance transformers in the WPDC and design parameters are summarized in Table 4.

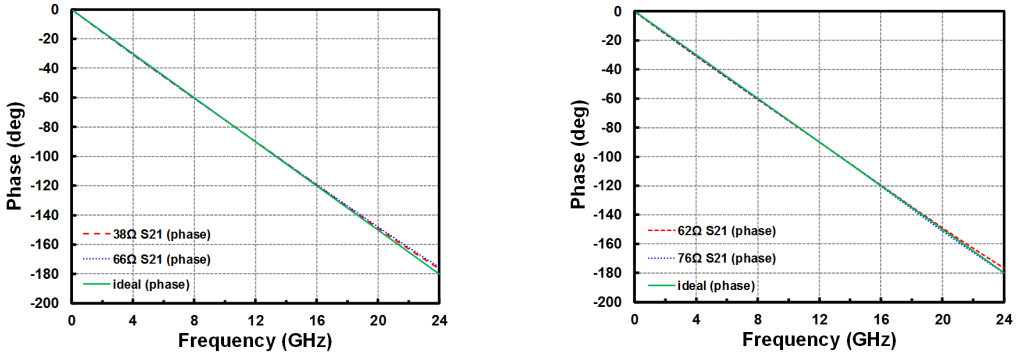
Table 4 – Design parameters of λ/4 impedance transformers in WPDC

Line width=7 μm line spacing = 5 μm	L1 (pH)	L2 (pH)	C1 (fF)	C2 (fF)
38Ω λ/4 transformer for WPC	230	154	84	55
62Ω λ/4 transformer for WPD	344	284	47	38
66Ω λ/4 transformer for WPC	366	302	44	36
76Ω λ/4 transformer for WPD	420	350	38	31



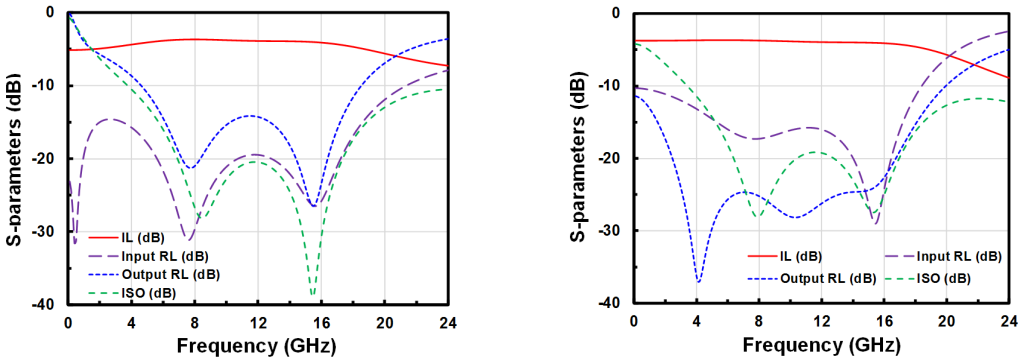
(a) (b)

Figure 29 – Simulated ILs (solid) and RLs (dotted) of (a) 38Ω (red) and 66Ω (blue) λ/4 transformers in WPC and (b) 61Ω (red) and 76Ω (blue) λ/4 transformers in WPD.



(a) (b)

Figure 30 – Simulated phase responses for (a) 38Ω (solid) and 66Ω (dotted) λ/4 transformers in WPC and (b) 61Ω (red) and 76Ω (blue) λ/4 transformers in WPD.



(a) (b)

Figure 31 – Simulated S-parameters of (a) the two-section lumped-element Wilkinson power combiner and (b) the two-section lumped-element Wilkinson power divider.

Simulated S-parameters of 38Ω and 66Ω λ/4 transformers for Wilkinson power combiner (WPC) and 62Ω and 76Ω λ/4 transformers for Wilkinson power divider (WPD) were plotted in Figure 29. For 38Ω and 66Ω λ/4 transformers in the WPC, insertion losses (ILs) lower than 0.8 dB and return losses (RLs) higher than 14 dB at 20 GHz were observed. ILs lower than 1.0 dB and RLs higher than 10 dB are satisfied from DC to 19.7-GHz for 62Ω and 76Ω λ/4 transformers in the WPD. λ/4 impedance transformers with higher characteristic impedance show narrower bandwidth than those with lower characteristic impedance due to the decrease in the cut-off frequency. The phase responses of the 38Ω and 66Ω λ/4 transformers, as shown in Figure 30 (a), are 90 degrees at 12 GHz and the phase deviation is within 3.2 degrees at 24 GHz. Figure 30 (b) shows the phases of 62Ω and 76Ω λ/4 transformers in the WPD and they are 90 degrees at 12 GHz. The phase deviation from the ideal T/L (green solid line) is less than 2.7 degrees at 24 GHz.

Simulated S-parameters of the WPC and the WPD are shown in Figure 31 (a) and Figure 31 (b), respectively. For the WPD, the minimum IL is 0.63 dB at 7.0 GHz and it is less than 2.0 dB from 1.0 to 18.0 GHz. RLs both at input (IRL) and an output (ORL) remain higher than 10 dB from DC to 18.4 GHz. Isolation (ISO) is higher than 10 dB from 3.2 to 24.0 GHz. The minimum IL of the WPC is 0.7 dB at 8.0 GHz and it is less than 2.0 dB from DC to 19.0 GHz. Both IRL and ORL of the WPC are higher than 10 dB from 4.0 to 18.0 GHz. Isolation (ISO) is higher than 10 dB from 4.0 to 24.0 GHz. The relatively narrow bandwidth of the WPC compared to the WPD can be attributed to the difference in the impedance transformation ratio. The simulation results demonstrate that the proposed novel design method is feasible in implementing a highly efficient, wideband lumped-element WPDC in a small for- factor.

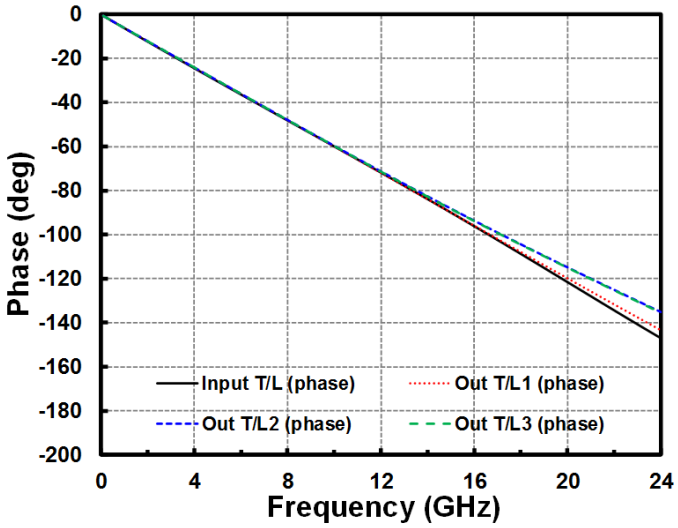


Figure 32 – Simulated phase responses of the input (solid) and output T/Ls (dotted).

Next, phase responses of the input T/L and the output T/Ls are simulated and those results are plotted in Figure 32. The value of inductances and capacitances for each T/L are determined based on Equation 17 and Equation 18 at 12 GHz and those values are summarized in the table in Figure 26. The phase synchronization between the input T/Ls and the output T/Ls is achieved at 12 GHz and it is 72 degrees. The phase deviation between the input T/L and the output T/L_1 is 2 degrees at 20 GHz, but that between the input T/L and either the output T/L_2 or T/L_3 is up to 7 degrees at the same frequency. This would be caused by the difference in the number of turns in symmetric inductors used for realizing each T/L. While the input T/L and the output T/L_1 are three turns symmetric inductors, the output T/L_2 and T/L_3 are two turns symmetric inductors. The higher number of turns essentially brings more inter-winding parasitic capacitance, which decreases the cut-off frequency of the artificial T/Ls and thus results in more phase delay at higher frequency. In order to alleviate this issue, the number of turns of symmetric inductors should be identical or set the higher frequency as a reference design point for the phase synchronization to reduce the phase deviation.

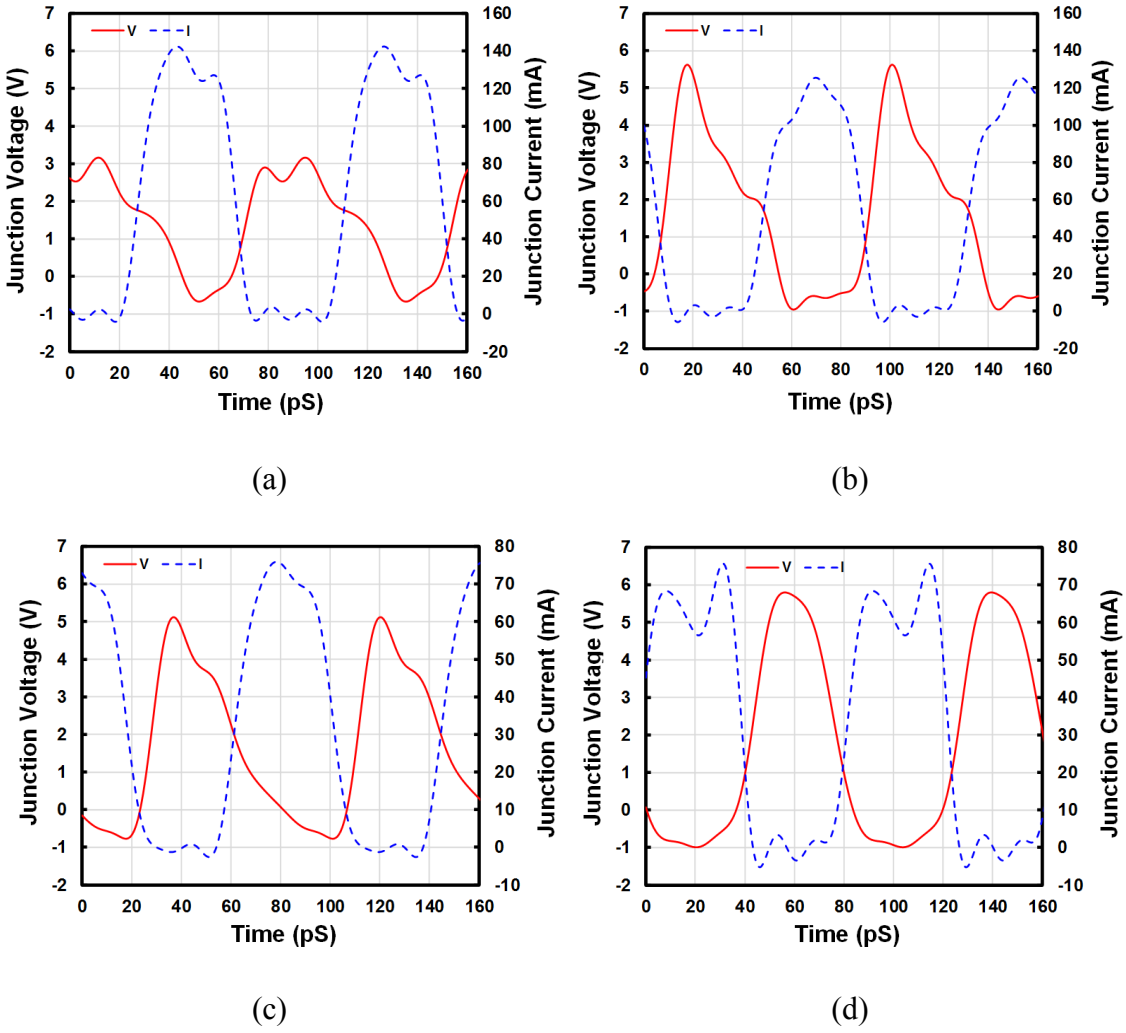


Figure 33 – Simulated time domain collector-base junction voltage and current waveforms of (a) the first stage, (b) the 2nd stage, (c) the 3rd stage, and (d) the last stage in the single DPA core at the input frequency of 7 GHz with 3.6 V supply.

The simulated time domain collector-base junction voltage and current waveforms of upper SiGe HBTs in cascode, from the first to the last stage of the single DPA core, are presented in Figure 33. The emitter current of the common base SiGe HBT is exploited as 1st order approximation of the junction current and it is reasonable to check safe operation of SiGe HBT cascode [56]. The voltage and current waveforms are obtained when the NDPA is saturated at 7 GHz with 3.6 V supply. Due to the dumping collector resistor terminated at the collector of the first stage, the half of its output power is dissipated as

heat and that is why the junction voltage swing is just half of those at other stages. Aside from the first stage, the junction current diminished to zero when the junction voltage swing is at its peak value, which means the SiGe cascode power cell would be protected from pinch-in effect and thermal runaway. Similar peak voltage and current swing per unit emitter area indicates that the designed output T/Ls achieves the power matching of each stage well. Figure 33 (a) also shows that there is still a voltage headroom for enhancing the output power of the first stage by employing supply scaling technique [94] to the NDPA.

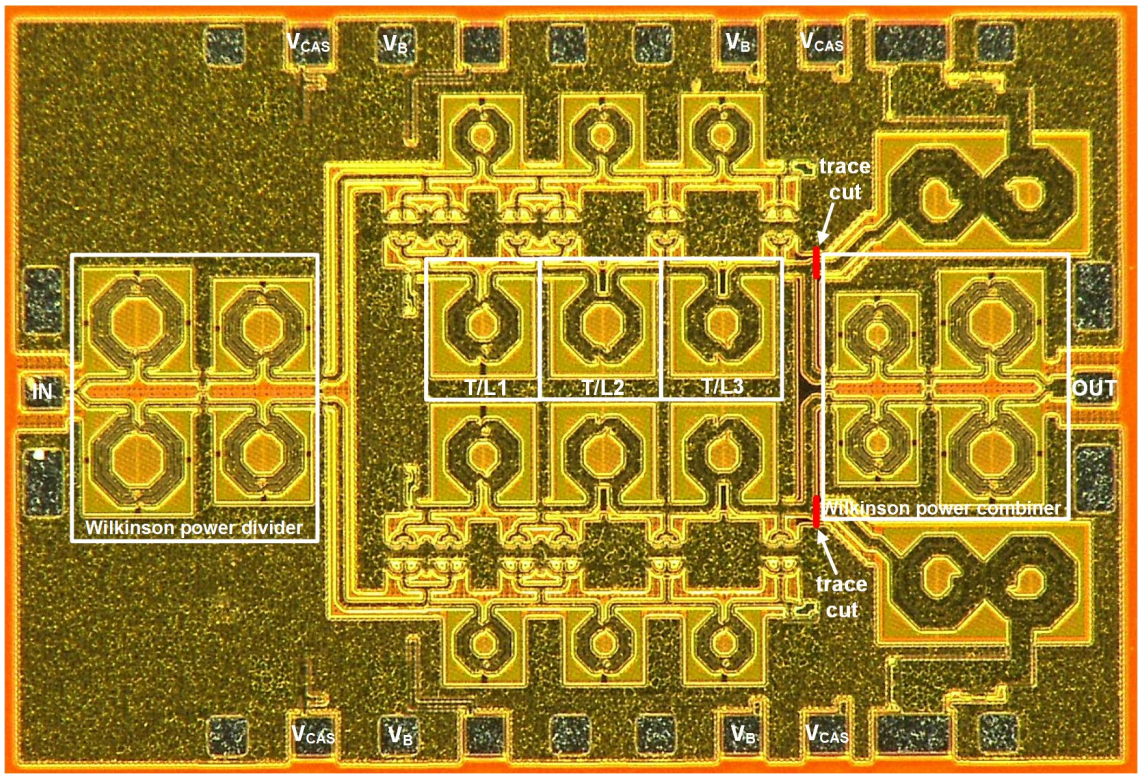


Figure 34 – Microphotograph of the fabricated 2-19 GHz SiGe HBT NDPA. Red lines are places where metal traces are cut by laser trimming.

A prototype is fabricated in GlobalFoundries 0.12-μm SiGe 8HP BiCMOS technology, which features peak f_T/f_{max} of 220/280 GHz and BV_{CEO}/BV_{CBO} of 1.8/6.0 V. A chip photograph of the NDPA is depicted in Figure 34 and realized in a 1.9 x 1.3 mm^2 active area. On-wafer measurement is performed. On-die RF chokes were disconnected by

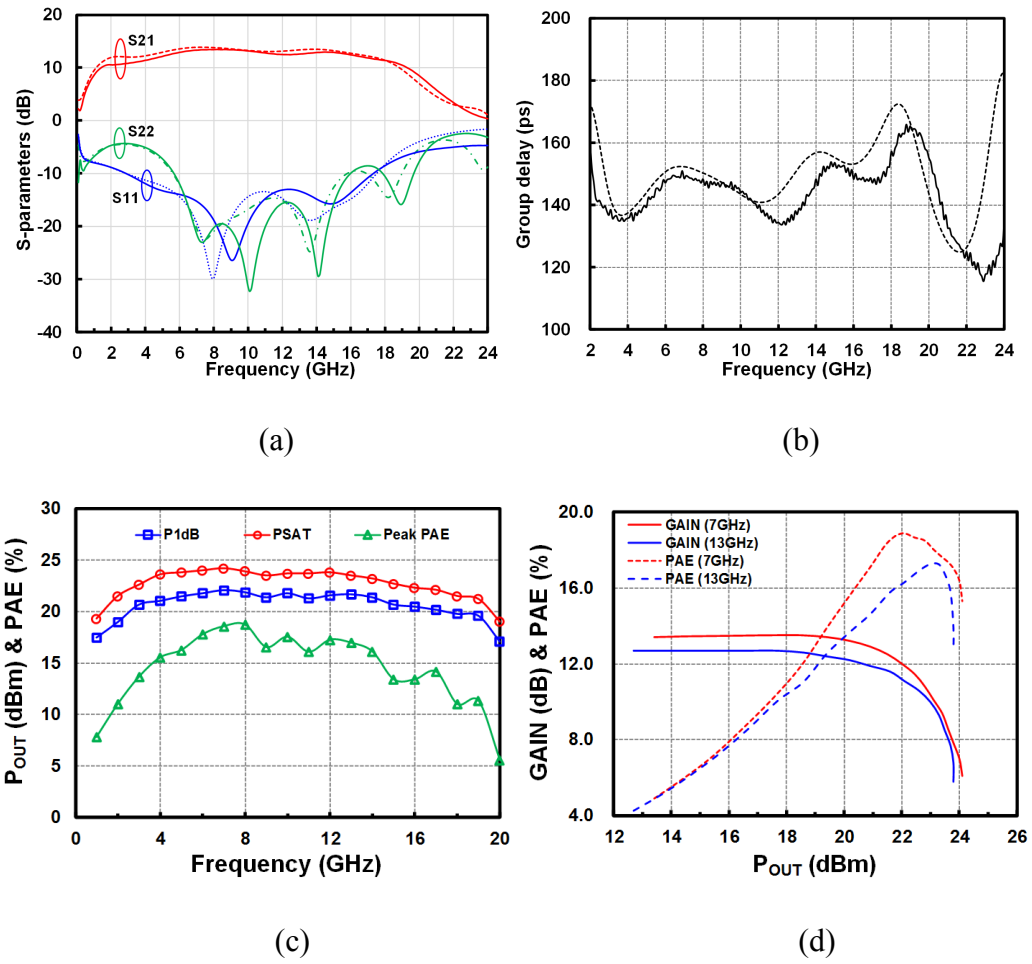


Figure 35 – (a) Measured (solid) and simulated (dotted) S-parameters of the NDPA (b) group delays (c) measured P_{1dB}, P_{SAT}, and peak PAE with input frequency sweep and (d) P_{OUT} and PAE at 7 and 13 GHz with an input power sweep.

laser trimming, and an external bias-tee is used to ensure that the chokes did not limit the measurement bandwidth. A quiescent current is 94 mA at a 3.6 V supply, with V_B=0.84 V and V_{CAS}=1.9 V.

Figure 35 (a) shows simulated and measured S-parameters of the NDPA. The peak gain is 13.5 dB at 8 GHz, with 3 dB bandwidth from 1.8 to 19.1 GHz. IRL and ORL are higher than 10 dB from 1.7 to 17.4 GHz and 5.5 to 19.5 GHz, respectively. Figure 35 (b) show the group delay of the NDPA. It has 36 ps variation from DC to 20.0 GHz, which is sufficient to support a 10Gb/s PRBS signal. Such variation in the group delay would stem

from the Chebychev WPDC design, which has unavoidable internal reflection between the impedance transformers and hence results in higher phase distortion. To reduce the group delay variation, WPDC will be designed based on "Maximally flat", not "Chebyshev" coefficients at the cost of reduction in the impedance matching bandwidth.

For large signal performance characterization, cable losses were compensated carefully using a CW signal generator and power sensor/power meter. At first, the proposed NDPA was characterized with the input frequency variation, as shown in Figure 35 (c). Peak P_{SAT} and P_{1dB} are 24.2 dBm and 21.7 dBm, respectively, with peak PAE of 19%. A 3dB P_{SAT} and P_{1dB} bandwidth is from 2.0 to 19.0 GHz, with PAE higher than 11%. Figure 35 (d) shows power gain and PAE of the NDPA, with the output power sweep at two frequencies. P_{SAT} and P_{1dB} are 23.9±0.3 dBm and 21.5±0.2 dBm, respectively. Power gain and peak PAE are higher than 12.7 dB and 17%, respectively.

The test setup for eye diagram measurement is described in Figure 36. For the eye diagram test, 2.5 and 3.5 Gb/s OOK modulated signals on a 6 GHz carrier frequency were synthesized using an arbitrary waveform generator (Tek 70002A), amplified by an external amplifier (SHF_807), and then applied to the NDPA input. The NDPA output waveform was captured by a real time oscilloscope and demodulated offline in MATLAB. Attenuators at the input and output of the NDPA are exploited to control the output power and to protect the oscilloscope from the high voltage swing. Clear eye openings, as depicted in Figure 37 (a) and (b), demonstrate the broadband amplification capability of the NDPA. Due to the limited bandwidth of the AWG (it only supports up to 10 GHz), it was not possible to synthesize higher data rate signal, but 3.5Gb/s OOK modulated signal still indicates the wide bandwidth of the proposed NDPA.

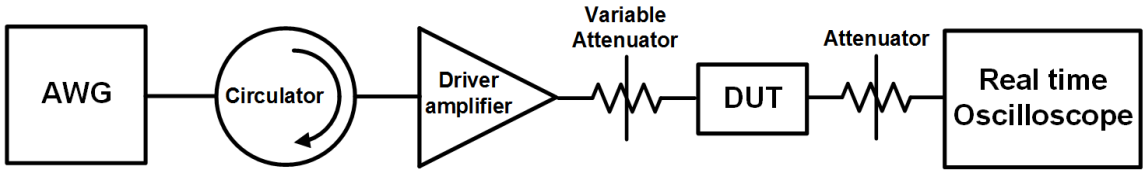
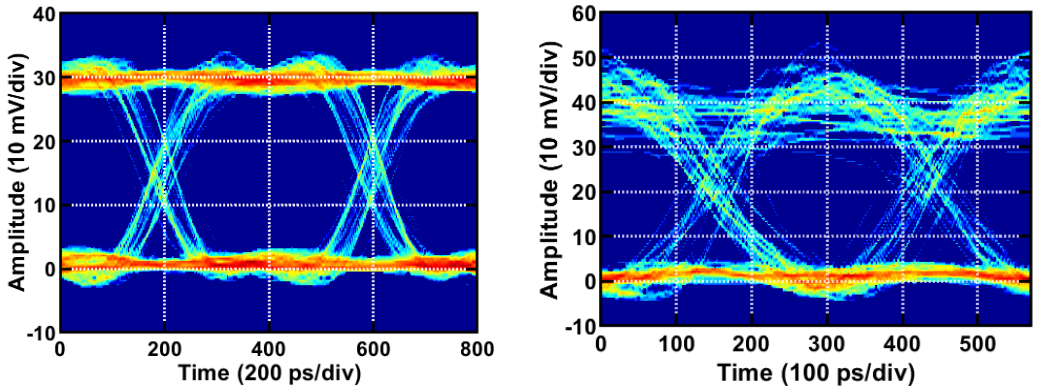


Figure 36 – Simplified block diagram of the eye diagram test setup.



(a) (b)

Figure 37 – Eye diagrams of OOK demodulated signals at the NDPA output for (a) 2.5 Gb/s and (b) 3.5 Gb/s data rates.

Table 5 summarized state-of-the-art Si-based broadband DPAs. The proposed NDPA with the novel compact and wideband lumped-element WPDC demonstrates the highest P_{OUT} with similar or wider bandwidth among any Si-based DPAs. Thus, it would pave the way for developing Si-based high power broadband amplifier.

Table 5 – Comparison of State-of-the-art Si-based Distributed PAs

	[86]	[85]	[95]	[87]	**This work**
Technology	130 nm Bulk CMOS	45 nm SOI CMOS	90 nm SiGe BiCMOS	0.25 μm SiGe BiCMOS	120 nm SiGe BiCMOS
Topology	Four-stacked, Uniform	Four-stacked, Uniform	Four-stacked, Uniform	Two-stacked, Uniform	Cascode, Non-uniform
Supply (V)	3.5	4.4	5.0	5.0	3.6
BW (GHz)	2 - 16	1 - 17	1-20	1 - 12	2 - 19
P_{SAT} (dBm)	18.5	21.0	19.5*	20.0	24.2
P_{1dB} (dBm)	15.5	18.2	-	17.5	21.7
PAE (%)	17.0	19.0	18.5**	22.1	19.0
Gain (dB)	10.0	17.1	14.0	12.0	13.4
Size (mm^2)	0.83	1.14	2.54	2.10	2.47

CHAPTER 5. DESIGN OF HIGHLY LINEAR SIGE HBT POWER AMPLIFIER FOR 802.11AC/AX WLAN

Increasing demand on high speed mobile access requires a spectrum-efficient wireless connectivity platform. With dense modulation and MIMO technique, 802.11ac WLAN standard has been widely deployed as a viable solution [96]. Even with such a successful settlement of 802.11ac WLAN for indoor wireless communication, tremendous users in a dense environment will degrade the quality of wireless connection and lower actual data throughput. To address those issues, 802.11ax WLAN [97] is emerged and it has recently been approved by Federal Communications Commission (FCC) as the next generation WLAN. Compared with 802.11ac WLAN standard, the new 802.11ax standard has many benefits. First, 802.11ax supports 8 x 8 multi-units MIMO downlink (DL) and uplink (UL), which leads to four times higher data throughput than 802.11ac with 2 x 2 MIMO. Second, OFDMA is proposed for allocating users with different overhead to a channel to improve user experience. UL resource scheduling is for increased capacity, better user experience in a dense environment, and better battery life by reducing a PA turn on time. A four times longer OFDM symbol enables to increase efficiency and support higher data rates. The most importantly, utilizing 1024 QAM will increase network capacity by 25% compared with 802.11ac with 256 QAM. Even though all mentioned characteristics will be prospective, but they would not come without any cost. The more dense modulation scheme, the 8 x 8 MIMO technique, and the longer OFDM symbol all together will put PA designers tougher situation due to an electrical-thermal induced linearity degradation. As 802.11ac/ax impose stringent linearity requirements on power

amplifiers due to a high peak-to-average power ratio signal, operation at large back-off and PAE reduction are unavoidable. As a result, III-V processes have dominated the development of high output power (P_{OUT}) WLAN PAs [98, 99].

To replace them with lower cost Si-based PAs, several linearity enhancement techniques have been proposed, such as digital pre-distortion (DPD) or a spatial power combining, at the cost of increased complexity in digital domain [100, 101]. In addition, multiple analog linearization techniques were presented; one of which is to exploit a PMOS varactor at the gate of a NMOS transistor for AM-PM compensation [40] and another is to use a FET switch as a variable resistor in a RC feedback to compensate for AM-AM [102]. As the PMOS varactor capacitance is added to the gate of the NMOS FET, it would make an inter-stage matching between a stage and its subsequent stage difficult to cover 5-6 GHz band. The active feedback linearizer forces to use a low resistance in the RC feedback, which results in the reduction of the power gain of the output stage and thus PAE as well. A 2nd harmonic short is used for linear class-AB PAs [41, 103], but an inductor on supply lane occupies Si area and causes ohmic losses, degrading both output power and efficiency. SiGe HBTs [104, 105] are suitable for WLAN PAs due to their capability for high power density, ruggedness, and CMOS compatibility. The linearity of SiGe HBTs can be degraded, however, due to a current gain (β) decrease resulting from a junction temperature (T_J) rise, which will inevitably degrade EVM.

Not only the electrical point of view, but also the thermal property of SiGe HBTs must be taken into account in the linear PA design. [106] used the mixed-mode device and circuit simulation to examine how a self-heating transient of a CMOS FET has impact on the PA electrical performance and proposed an adaptive gate biasing scheme to minimize

it. As introduced in the chapter 1.3, the mutual thermal coupling as well as the self-heating of a SiGe HBT array increase their junction temperature, which results in a unavoidable current gain (β) drop and leads to an early power gain compression [107]. Without proper temperature compensation, the collector current would be concentrated at a center npn sub-collector in the SiGe HBT array and it increases rapidly. As a result, f_T/f_{max} and β of the SiGe HBT array are decreased due to Kirk effect and its elevated junction temperature. To prevent this adverse effect, base or emitter ballasting resistors [108] are used for any HBT PA at the cost of reduced voltage headroom and power gain.

Another important design concern in WLAN PAs is its dynamic operation. Alternative turning the PA on and off induces an electro-thermal transient response issue and it is related with a finite thermal time constant (τ_{TH}) of the PA, briefly introduced in the chapter 1.3. τ_{TH} is the amount of time it takes to heat up a specified volume of a material to 63.2% of the steady state junction temperature. Depending on the amount of the power dissipation as heat and the temperature difference between a heat source and a heat sink, it usually takes for an output stage more than a few seconds to reach its thermally steady state. In other words, the PA never reaches its thermally steady state for the dynamic operation. For this reason, the notion of dynamic EVM (DEVM) [109] is more realistic than static EVM in evaluating WLAN PA's in-band linearity. [110] investigated how does this electro-thermal transient has impact on the minimum DEVM floor and it is quantified using Equation 19.

$$\mathrm{DEVM_{dB}} = 20\log(G_{max} - G_{min}) \tag{19}$$

where G_{max} and G_{min} are the power gain when PA is off and on, respectively. It is predicted from Equation 19 that the gain difference must be less than 80 mdB to satisfy the DEVM floor of -40 dB, which would be the minimum requirement of 802.11ax operation. As explained, the gain deviation will be larger with the longer data burst (up to 4 ms) for 11ax operation. The 8 x 8 MIMO will have higher ambient temperature than its 4 x 4 counterpart and thus this thermal-electrical transient can be a severe issue in designing highly linear SiGe HBT PA. Therefore, careful electro-thermal design approach is required to realize 802.11ax operation. To alleviate this, PTAT current source at a driver stage can be used to compensate for the temperature-induced power gain variation.

To address these challenges, a highly linear, high-power SiGe HBT PA supporting both 802.11ac and 802.11ax WLAN standards is presented in this chapter. Both P_{OUT} and PAE are improved by proposing a novel compact, highly efficient 2nd harmonic-shorted four-way output transformer balun. A chapter 5.1 deals with its design procedure in stages. Moreover, a temperature-compensated dynamic bias circuit with embedded thermal sensors is designed to manage T_J of SiGe HBT power arrays, which helps prevent premature AM-AM compression. A novel layout-based thermal couple model is introduced in a chapter 5.2 to exactly account for the electrical-thermal effect in the PA design and then the correlation between the proposed bias circuit with its corresponding SiGe HBT power arrays is explained in detail for linear performance.

To sum up, the proposed highly linear, high power SiGe HBT PA demonstrated record linear power in 802.11ac/11ax WLAN compared to any Si-based competitors. Thus, it is strongly asserted that taking both electrical and thermal perspective will be important to draw full capability of SiGe HBT BiCMOS technology for the highly linear PA design.

5.1 Circuit Schematic of the Proposed Highly Linear SiGe HBT PA

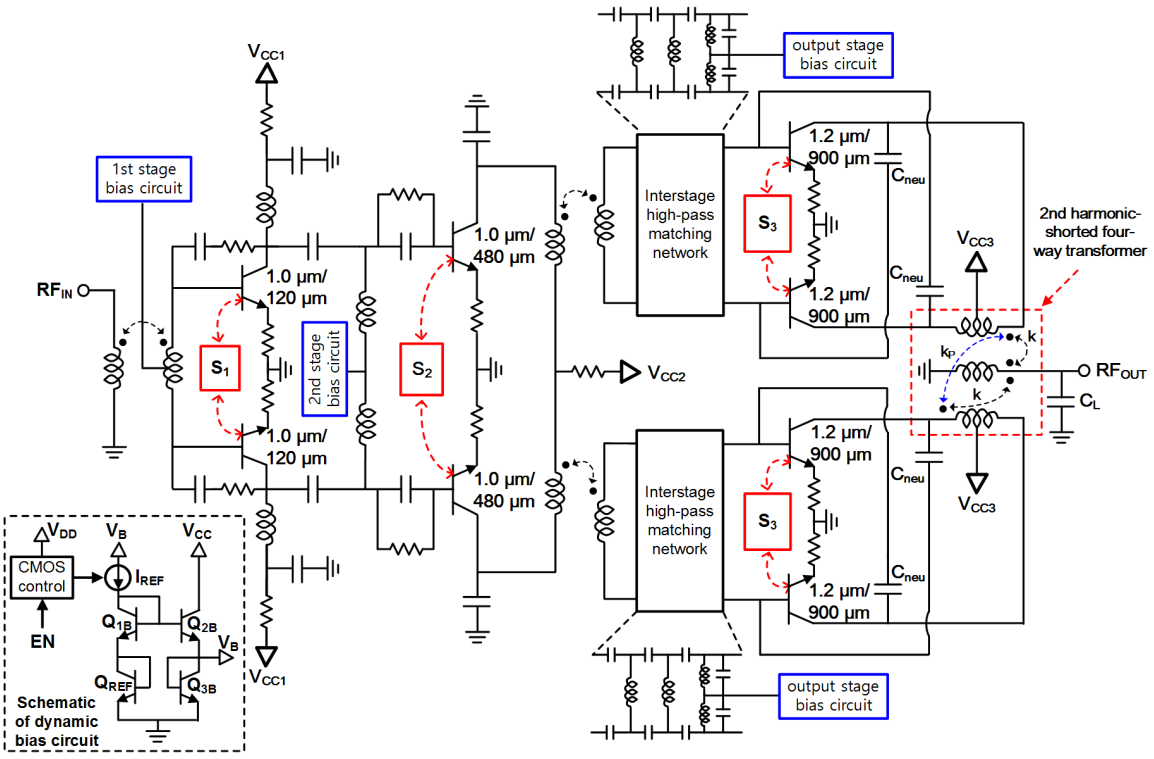


Figure 38 – Circuit schematic of the proposed 3-stage SiGe HBT PA with a compact 2nd harmonic-shorted four-way transformer (highlighted as red dotted box). The lower left inset shows a schematic of an on-chip temperature compensated dynamic bias circuit with an embedded thermal sensor (Q_{REF} is indicated as S_1, S_2, and S_3).

Figure 38 shows a circuit schematic of the SiGe HBT PA. It is 3-stage and the emitter area ratio between one stage and a subsequent stage remains about 4 for linear operation. All SiGe HBT array transistor consists of multiple sub-collectors (the number of sub-collectors for 1st stage, 2nd stage, and the output stage are 3, 5, and 10, respectively) with three emitter stripes considering tradeoff between power density and junction temperature. Sub-collector to sub-collector spacing in a SiGe HBT array is determined to be 5 μm to reduce mutual thermal coupling effect. The only the output stage has an emitter width of 1.2 μm to increase power density of the SiGe HBT array, which reduces a phase deviation caused by interconnect parasitic. The bias of each stage is from class-A to deep

class-AB to obtain both linear and highly efficient operation. Low parasitic inductance through-wafer vias (TWVs) are utilized for robust backside ground connection.

As indicated in an inset of Figure 38, a temperature-compensated dynamic bias circuit is composed of a current source (I_{REF}) with a 3.3 V CMOS enabled control logic and a SiGe HBT current mirror (Q_{1B} and Q_{2B}) with diodes (Q_{REF} and Q_{3B}). Only Q_{REF} (S_1, S_2, and S_3) is thermally-coupled to the corresponding SiGe HBT arrays and the operation principle will be shown in the next chapter with the aid of the layout-based thermal coupling model. Enable pulse (EN) is applied to the PA for dynamic operation.

A compact input transformer balun is realized for equal power splitting with 180° phase shift, and an inter-stage transformer is designed to generate two differential signals for driving the output stage. The design of the two transformers, specifically focused on the compact input transformer, will be shown in the next chapter. A multi-section high-pass matching network is inserted between the 2nd stage and the output stage to compensate for gain roll off at higher frequency band. Neutralization capacitors [111] (C_{neu}=0.73 pF) are used at the output stage to mitigate the Miller effect and stabilize the PA. Emitter ballasting resistors, decided based on $1\Omega\cdot\mu m^2$ (it is inversely proportional to the total emitter area of a SiGe HBT array), are inserted to all emitter of SiGe HBT arrays to prevent thermal runaway at elevated junction temperature. Series resistors are put on supply rails of the input and 2nd stage not only to stabilize the PA, but also to ease the inter-stage matching by lowering the optimum impedance of each stage. RC staggered bypass networks [112] are inserted at collectors of the 2nd and 3rd stages to suppress an even mode oscillation that would be caused by a resonance between a parasitic capacitance and a parasitic inductance of TWVs. EMX® was used for full 3D EM simulations.

5.2 Design of A Compact and Low Loss Four-Way Output Transformer Balun with Built-In 2nd Harmonic Short Impedance Termination

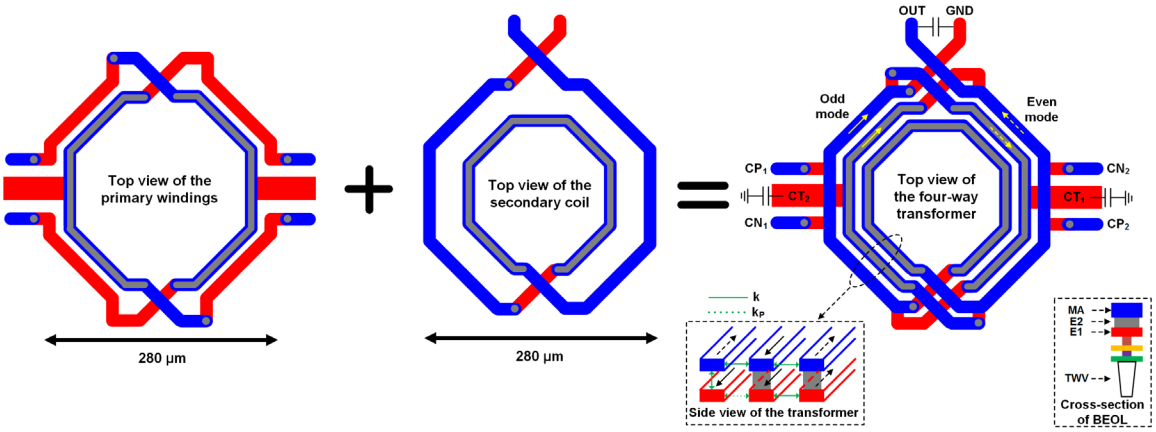


Figure 39 – Top view layout of the proposed built-in 2nd harmonic-shorted four-way output transformer balun. Implementations of two primary coils (left), a secondary winding (center), the four-way transformer (right) are shown graphically. The right corner inset indicates a cross section of back-end-of-line (BEOL).

Details of the proposed 2nd harmonic-tuned four-way output transformer are illustrated in Figure 39. It is made of two primary coils and a secondary winding, all within a single footprint and its diameter is just amount to 280 μm. While each primary winding has turn ratio of 1, the secondary coil's turn ratio is 2 to obtain desired impedance transformation ratio. A unique feature of back-end-of-line (BEOL), highlighted as dotted box in the Figure 39, is that it not only provides a 4 μm thick aluminum layer (MA) and a 3 μm thick copper layer (E1), but also offers a continuous-run copper via (E2). This E2 layer can be exploited to connect MA and E1 layers and as an additional metal stack layer, which would be beneficial in designing novel passive structures. Another key advantage of the BEOL lies in its high resistivity substrate. The resistivity of 1kΩ·cm Si substrate will be excellent advantage over its low resistivity counterpart (it usually around 10Ω·cm) since the substrate loss can be ignored for various passives design.

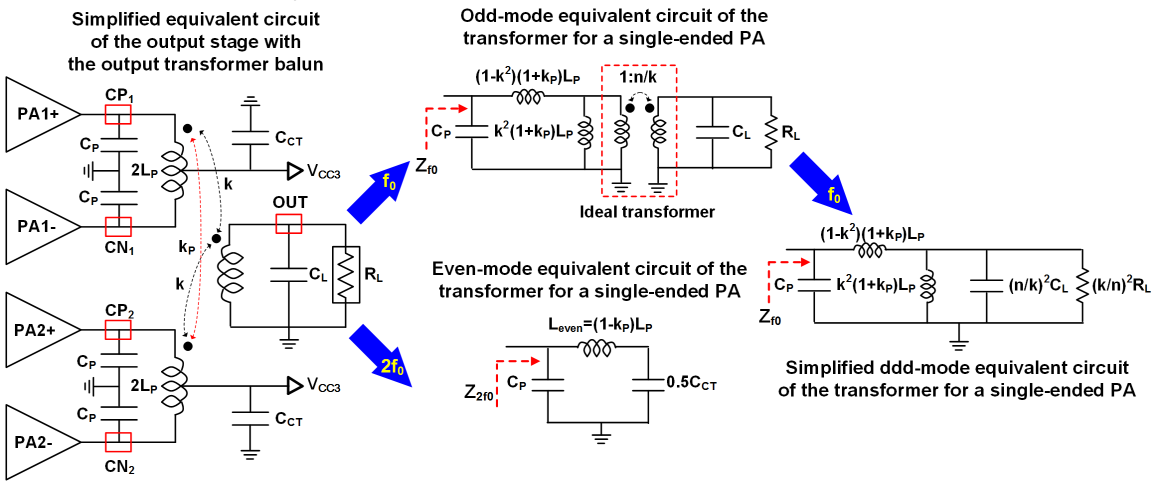


Figure 40 – Equivalent circuits of the output stage (left), the single-ended PA in odd-mode with the load at the secondary side (center top), the single-ended PA in odd-mode with the load shifted to primary side (right), and the single-ended PA in even-mode (center bottom).

The center and the innermost traces are a multi-layered stack connected through E2. With this scheme, both broadside and lateral magnetic coupling among the primary windings and the secondary coil are obtained, leading to high magnetic coupling factor k of 0.82, with a turn ratio (n) equal to 1.9. The multi-layered configuration has the two primary coils 4 μm apart, which results in a high primary-to-primary magnetic coupling factor (k_P) of 0.53. Consequently, a large primary inductance modulation (IM) can be attained, depending on desired mode of operation, which enables separate impedance matching at fundamental and 2nd harmonic frequencies. The IM of 3.24 can be obtained based on Equation 20 as below.

$$IM = \frac{1 + k_P}{1 - k_P} \tag{20}$$

In odd-mode, ac currents on the primary coils flow in the same direction, increasing a physical primary inductance (L_P) of 254 pH to an equivalent primary inductance $(1+k_P)L_P$

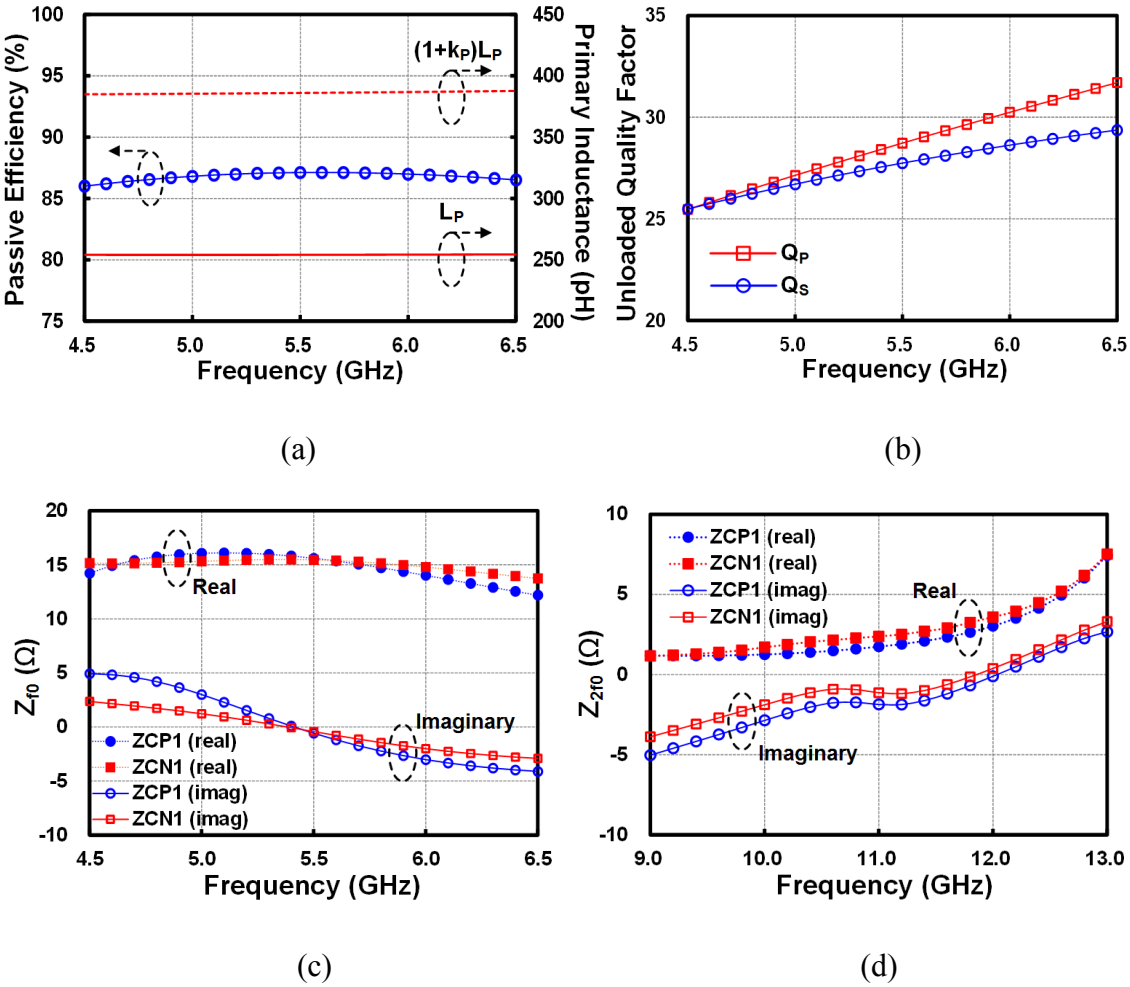


Figure 41 – Simulated (a) passive efficiency of the transformer (symbol) and primary inductance with (dotted) and without (solid) k_P effect, (b) quality factors of the primary (square) and secondary (circle) windings, (c) fundamental impedances, and (d) impedances at 2nd harmonic frequency.

equal to 388 pH, followed by enhanced quality (Q) factor of 28.8 at 5.5 GHz, as depicted in Figure 41 (a) and (b), respectively. A odd-mode equivalent circuit of the transformer for a single-ended PA is shown in Figure 40 and it is composed of a leakage inductance $(1-k^2)(1+k_P)L_P$, a magnetizing inductance $k^2(1+k_P)L_P$, a PA parasitic capacitance C_P, and an equivalent load shifted to the primary side. This 4th-order passive network transforms the 50Ω load to a 15.5Ω optimum impedance for a single-ended PA cell, which is equivalent to lowering the load to about 4Ω if the four PA cells is regarded as a unity PA cell.

In contrast, the even-mode primary inductance $L_{even} = (1-k_P)L_P$ is reduced to 119 pH due to a magnetic flux cancellation from the opposite current flow on the primary windings. As shown in an even-mode equivalent circuit in Figure 40, a MIM capacitor $C_{CT} = 3.4$ pF at each center-tap (CT_1/CT_2) of the transformer synthesizes a highly capacitive pi-network, resulting in a very low 2nd harmonic impedance. Because MIM capacitors at the center-taps must be grounded through TWVs, parasitic inductances of TWVs were taken into consideration in obtaining the desired 2nd harmonic impedance. Full 3D EM simulation including TWV effects was performed using EMX®. The metal line width of primary windings and the secondary coil is determined to be 16 μm to follow by electro-migration rule at the temperature of 125°C.

Figure 41 (a) shows simulated passive efficiency of the proposed four-way output transformer balun. The peak efficiency of 87.2% is observed at 5.5 GHz and it maintains 86.0% from 4.5 to 6.5 GHz. Simulated odd-mode ($Z_{OPT,f0}$) and even-mode ($Z_{OPT,2f0}$) impedances are plotted in Figure 41 (c) and (d), respectively. Real and imaginary part of fundamental impedance ($Z_{OPT,f0}$) are 15.4 ± 0.6Ω and 0 ± 3.5Ω, respectively, from 5.0 to 6.0 GHz. Real and imaginary part of 2nd harmonic impedance ($Z_{OPT,2f0}$) are 2.4 ± 1.1Ω and -1.5 ± 1.5Ω, respectively, from 10.0 to 12.0 GHz.

The simulation results demonstrate that the proposed four-way output transformer successfully achieves simultaneous fundamental and 2nd harmonic impedance matching without any additional inductor, with the efficient parallel power combining capability. It also enables a large impedance transformation ratio higher than 10:1 using a single inductor footprint, which will be difficult to obtain if a single section lumped-element matching network is used.

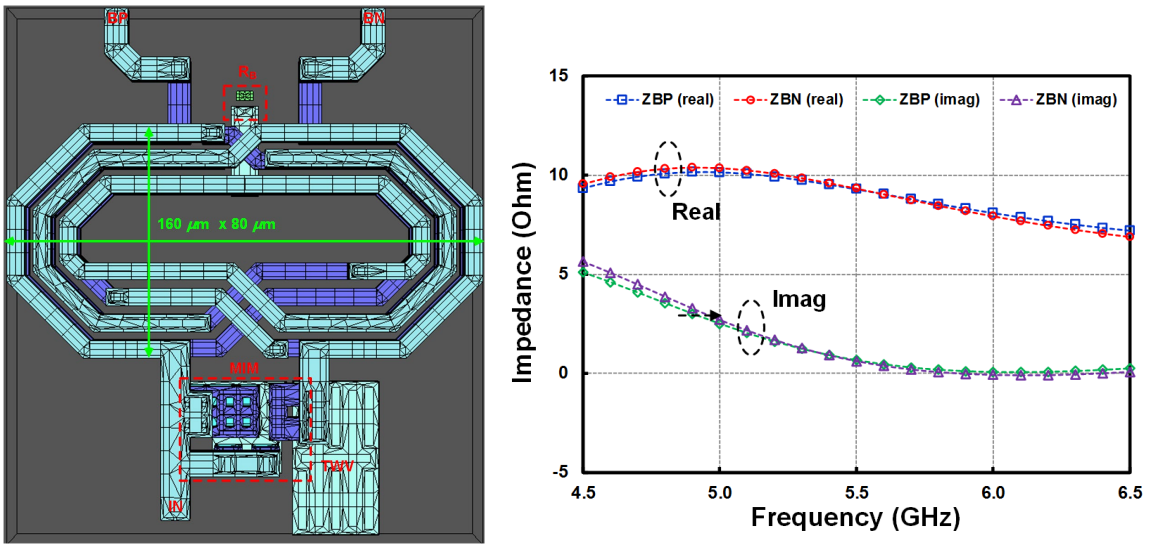


Figure 42 – Top view of the ultra-compact input transformer (left) and its simulated impedance plot (right).

To make the PA fully singled-ended operation, an input transformer balun is designed. The balance of a differential signal is regarded as the most important design parameter in the differential operation since amplitude and phase mismatches in the differential signal would induce the performance degradation, especially at the output stage and an even mode instability as well. The structure of the proposed ultra-compact input transformer balun is shown in Figure 42. Its physical size is just 160 μm x 80 μm thanks to both vertical and lateral magnetic coupling as achieved in the four-way output transformer balun. A MIM capacitor of 800 fF is added at a 50Ω source impedance for the optimum input impedance matching. A 4 Ω series resistor is inserted at a center-tap of the input transformer to suppress an even mode oscillation. The metal line width is chosen to be 6-μm to minimize capacitive coupling between the primary and the secondary windings, which is the main cause of the signal imbalance. Using the narrow metal line width also increases the ohmic loss of the input transformer, but it is not critical as such in the output transformer since it hardly affects the overall efficiency of the 3-stage PA.

Simulated impedance looking into two outputs (BP/BN) of the transformer balun is plotted in Figure 42. The input capacitance of SiGe HBT arrays in the 1st stage were included in the simulation. The graph clearly shows that the proposed ultra-compact input transformer balun successfully transforms the 50Ω source impedance to the optimum impedance of 9 ± 1Ω from 5 to 6 GHz with the reduced imbalances both in the amplitude (real part) and the phase (imaginary).

5.3 Design of A Temperature Compensated Dynamic Bias Circuit with Integrated Thermal Sensors

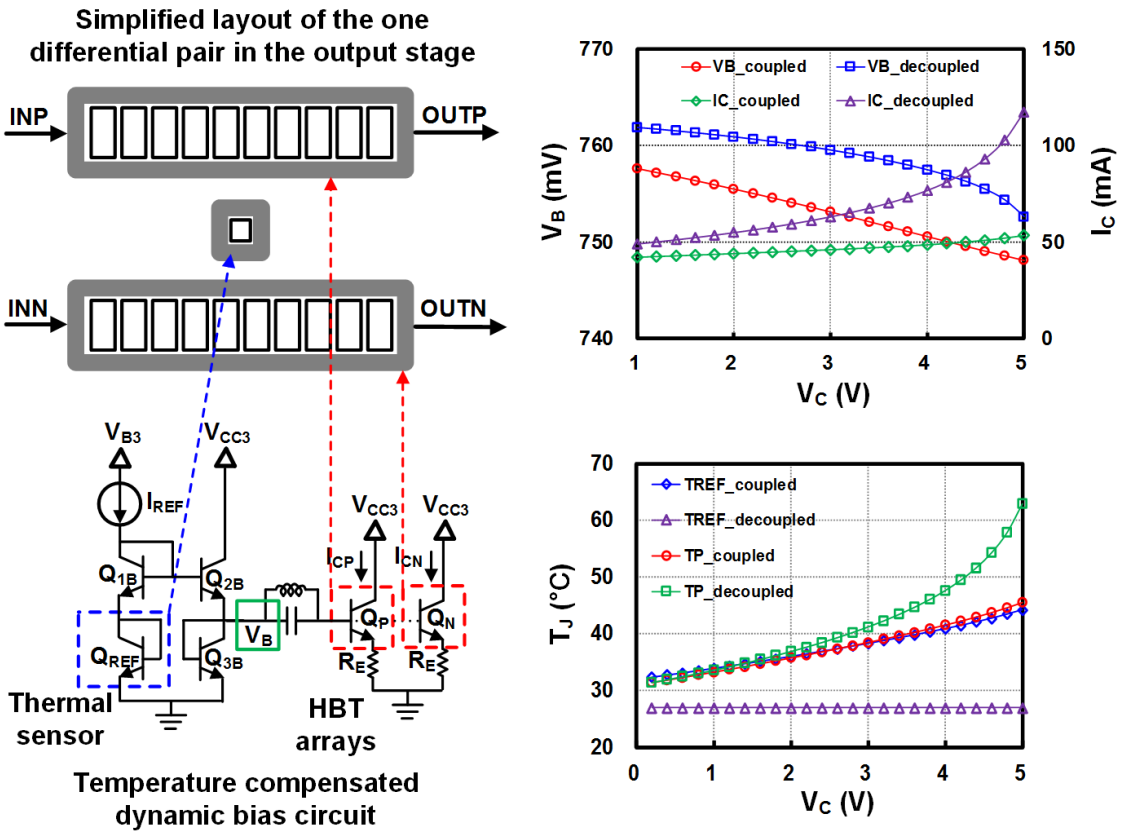


Figure 43 – Top view layout of the single differential pair in the output stage and its corresponding simplified circuit (left), DC base voltage and collector current of Q_P over collector voltage sweep with and without thermal coupling (right top), and junction temperature variation with and without thermal coupling (right bottom).

In this chapter, the only output stage's thermal characteristic is treated since it has much higher thermal time constant than other stages, and thus DEVM of the PA will be dominated by the thermal transient response of the output stage. The electro-thermal behavior of a single differential pair in the output stage is described in Figure 43. The thermal sensor Q_{REF}, which was indicated as S3 in Figure 38, is located between two SiGe HBT arrays Q_P and Q_N in a symmetrical fashion to sense and track their junction temperature. Other elements in the bias circuit are kept far away from Q_P and Q_N to minimize mutual thermal coupling. This layout strategy is important to prevent an overcompensation of thermally-induced collector current (I_C) increase, otherwise early gain compression occurs due to the rapid decrease in a base voltage (V_B).

At first, DC simulation is performed to check the functionality of the proposed bias circuit with the thermal sensor. The ambient temperature is at 27°C. Collector voltage (V_C) of Q_P and Q_N are swept from 1.0 to 5.0 V with and without thermal coupling between Q_{REF} and Q_P/Q_N to see how their I_C and junction temperature (T_J) change. As shown in a right top side plot in Figure 43, complementary to absolute temperature characteristic (CTAT) of the thermally-coupled diode Q_{REF} decreases V_B linearly with increased V_C in Q_P and Q_N, which helps to maintain their collector current and would prevent β reduction from T_J rise. A right bottom side graph clearly shows that T_J of Q_{REF} exactly follows that of Q_P, which proves that the integrated thermal sensor in the bias circuit is a simple and very effective method to prevent early AM-AM compression caused by the unavoidable T_J rise at high power operation of the SiGe HBT PA.

For large signal simulation, a novel layout-based thermal model provided by a process design kit is utilized and it is shown in Figure 44. For example, the location of npn

sub-collectors in SiGe HBT power arrays Q_P/Q_N and Q_{REF} (each npn sub-collector in HBT array is highlighted as a blue dotted box) are set with respect to the origin. Then the internal thermal model reflects not only self-heating of the SiGe HBT arrays, but also all mutual thermal coupling among them based on their x-y coordinates, specified as dotted "Red" box in the table. The output stage arrangement in the proposed differential PA will be better than its single ended counterpart (power cells are located close to each other) due to the larger distance between SiGe HBT arrays, which reduces a mutual thermal coupling. With this convenient thermal model, the accurate prediction of the electro-thermal behavior of the SiGe HBT PA is possible in the simulation, which would greatly reduce design risk.

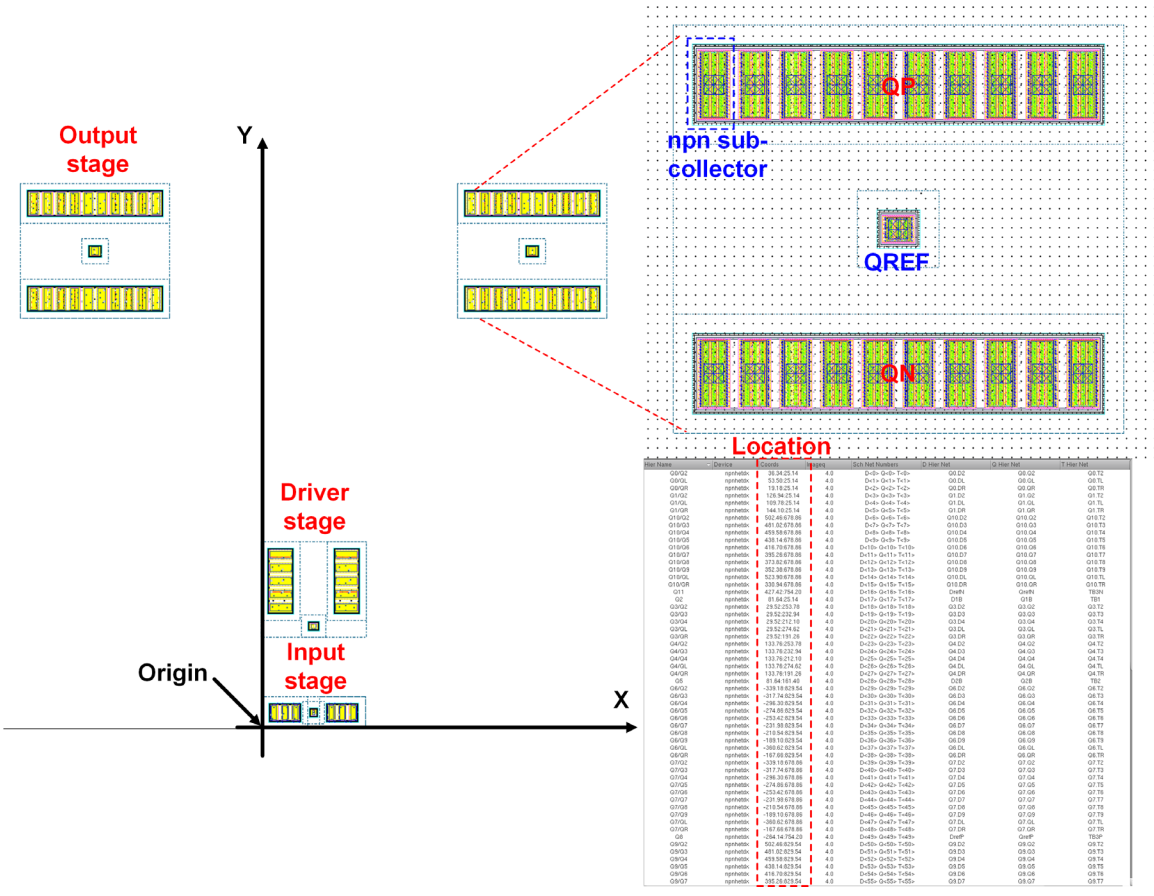


Figure 44 – Layout-based thermal model. Relative location of sub-collectors in SiGe HBT arrays in the layout are exploited to calculate the degree of the mutual thermal coupling among power cells as well as a self-heating themselves.

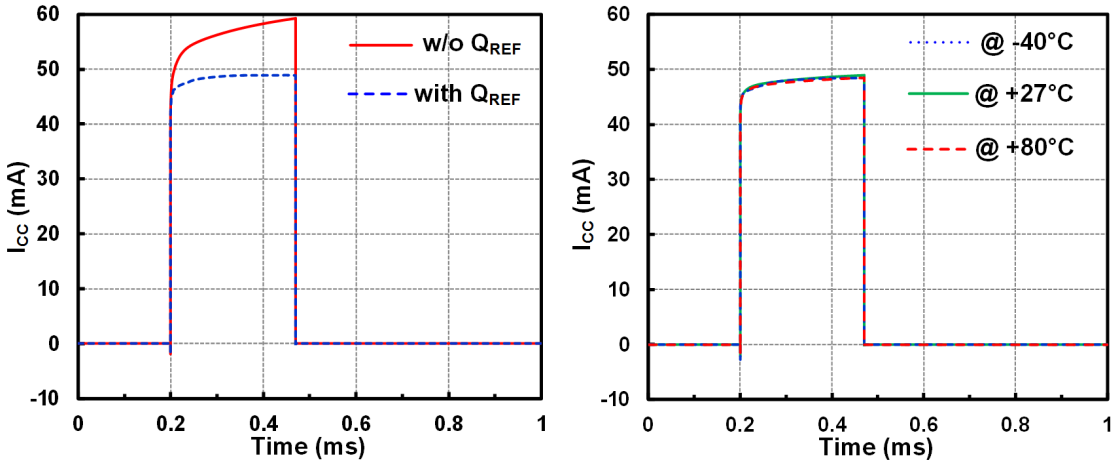
Large signal simulation results are summarized in Figure 46. The average temperature of Q_P is used for readability. As shown in Figure 46 (a), T_J of Q_P with the thermally-coupled Q_{REF} is lower by 12°C than thermally-decoupled case at 24 dBm. Compared with the DC simulation result, T_J tracking capability of Q_{REF} is relatively weaker for AC simulation case. There are two reasons for that. One is due to a thermal conductivity degradation in Si at high temperature [113]. This will reduce thermal coupling strength between Q_{REF} and Q_P/Q_N. Another is the non-uniform T_J distribution in the SiGe HBT array Q_P and Q_N under AC operation. Due to the cross thermal coupling among sub-collectors of the SiGe HBT arrays Q_P and Q_N, T_J difference will become large as P_{OUT} increases, which eventually reduces the thermal conductivity of Si substrate and the degree of the thermal coupling as well. The two mechanisms are correlated each other and thus proper value of emitter ballasting resistors must be determined based on the layout-based thermal model.

The memory effect is classified as static and dynamic (thermal). While static memory effect is related with the bandwidth of the bias circuit, dynamic memory effect is involved with the temperature mismatch between a reference and its corresponding power cell. Since varying V_B by sensing the junction temperature variation of the power cell is inherently closed-loop operation, the insufficient bandwidth of the bias circuit will cause static memory effect [114]. Figure 46 (b) shows a simulated normalized gain bandwidth of the bias circuit. The 1 dB normalized gain bandwidth of the bias circuit is about 300 MHz, which is 3.75 times of a 80MHz channel bandwidth for fast tracking of an instantaneous PA input signal amplitude variation.

Due to electrical-thermal feedback, the collector current of a SiGe HBT array is proportional to T_J of the device/T_J of the reference, as observed in Figure 43. To confirm

the electro-thermal transient response of the output stage, a pulsed operation of the thermally compensated dynamic bias circuit is simulated without a RF input excitation and those results are depicted in Figure 45. Figure 45 (a) clearly shows that the dynamic bias circuit with the thermally coupled Q_{REF} has less I_{CC} variation than that without the thermal coupling in the pulsed operation. In other words, the proposed PA in the dynamic operation would reduce a gain hysteresis when a pulse signal is at rising and falling edges [107], which would mitigate dynamic EVM (DEVM) degradation at high power.

The pulsed I_{CC} responses are obtained at various ambient temperatures of -40°C, +27°C, and +80°C, and those as plotted in Figure 45 (b). Thanks to the tight thermal coupling between Q_P/Q_N and Q_{REF} (center-to-center distance is about 70 μm), the collector current of the output stage is fairly constant regardless of its ambient temperature variation, which indicates the proposed PA with the thermally-compensated dynamic bias circuit would be robust to thermal memory effect.



(a) (b)

Figure 45 – Pulsed operation of a single differential pair in the output stage (a) with (dotted) and without (solid) thermal coupling to Q_{REF} and (b) the thermal coupling at various ambient temperatures.

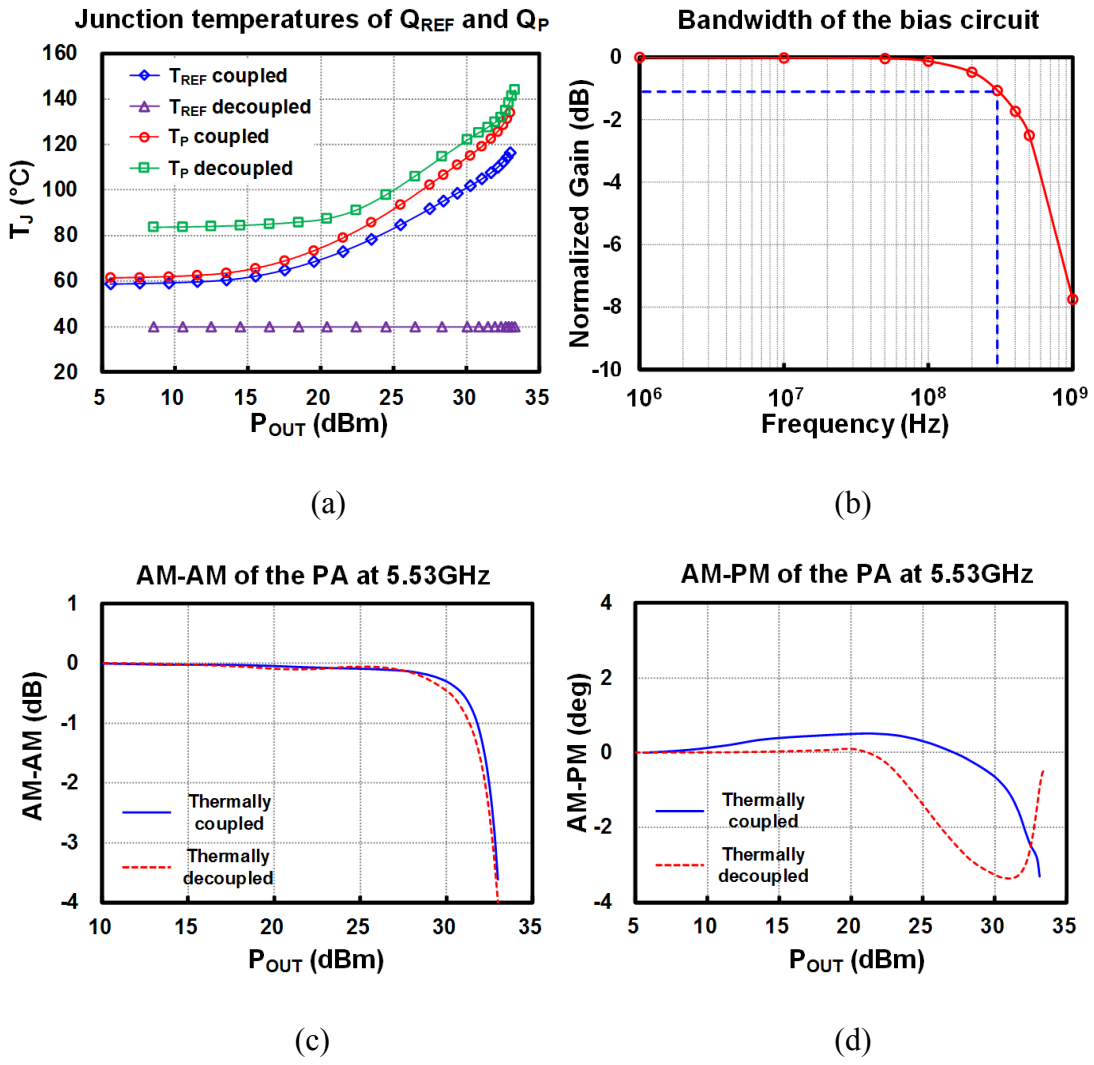


Figure 46 – Simulated (a) T_J of Q_{REF} and Q_P with and without thermal coupling, (b) normalized gain bandwidth of the bias circuit, (c) AM-AM with and without thermal coupling, and (d) AM-PM with and without thermal coupling.

Finally, both AM-AM and AM-PM simulations were carried out in Figure 46 (c) and (d). Simulated output P1dBs are 32.0 dBm and 31.2 dbm with and without thermal coupling between Q_{REF} and Q_P/Q_N, respectively. This would be attributed to β drop at high T_J. AM-PM is further distorted if Q_P/Q_N are not thermally-coupled to Q_{REF}. The abrupt phase lag at 20 dBm P_{OUT} is observed for thermally-decoupled case and it would stem from the increase of a diffusion capacitance at higher V_B. Thus, the optimal electro-thermal design would be of another key importance for highly linear, high-power SiGe HBT PAs.

5.4 Measurement Results and Discussion

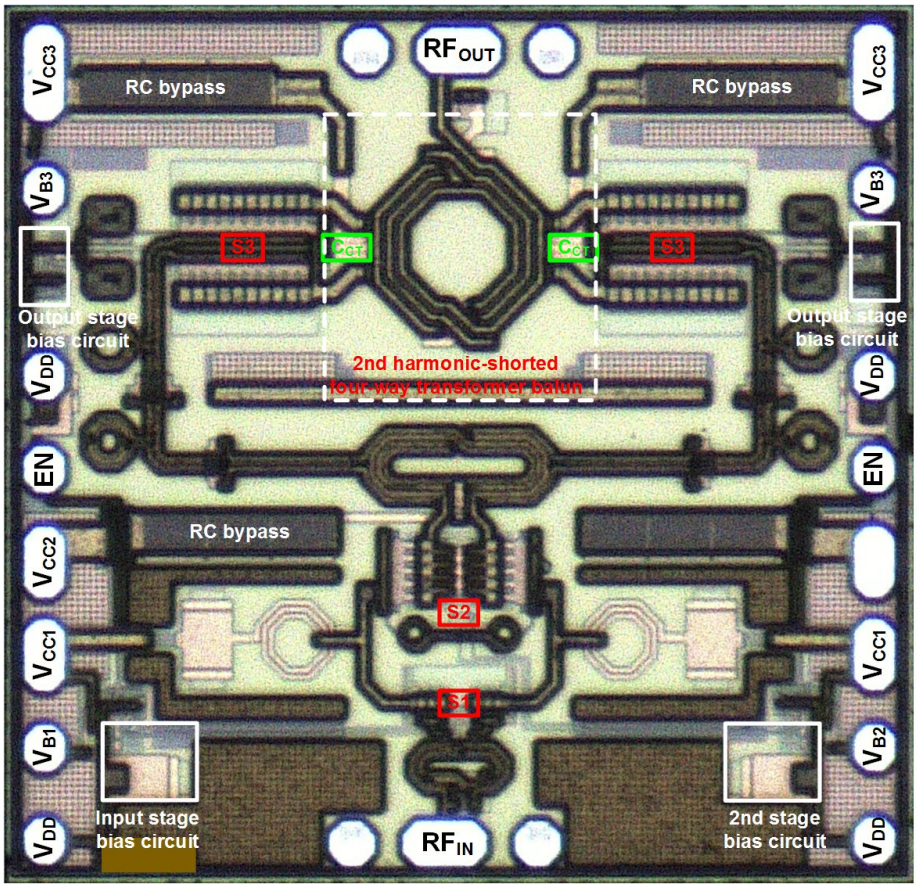


Figure 47 – Chip photograph of the proposed SiGe HBT PA.

A prototype was fabricated in GlobalFoundries SiGe BiCMOS 5PAX technology featured with peak f_T/f_{MAX} of 27/72 GHz and the 1kΩ·cm high resistivity substrate. The BV_{CEO} and BV_{CBO} of the SiGe HBT are 6.1 V and 17.7 V, respectively. The existence of the avalanche diode Q_{3B} in the dynamic bias circuit would extend collector-to-emitter voltage of a SiGe HBT beyond BV_{CEO}, making the PA robust under high voltage swing operation. The chip photograph of the PA is shown in Figure 47 and it is realized in a 1.45 x 1.40 mm^2 active area. A quiescent current is 225 mA on a 5 V supply. 3.3 V EN signal is applied to the CMOS control logic in the bias circuits for the dynamic operation of the PA. The bias circuits are kept far away from their corresponding power cells.

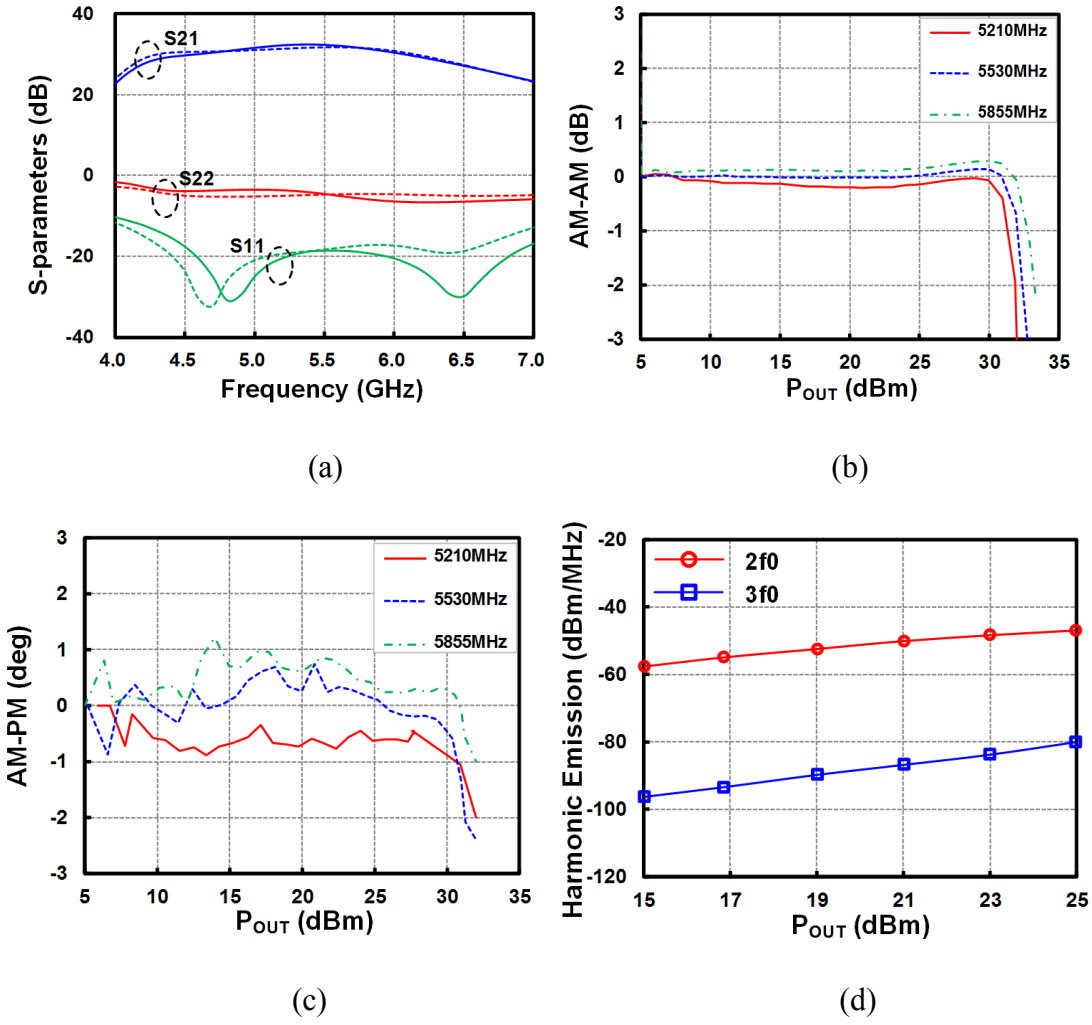


Figure 48 – Measured (a) S-parameters, (b) AM-AM at 10% duty cycle, (c) AM-PM at 100% duty cycle, and (d) harmonic emissions at $2f_0$ and $3f_0$ frequencies.

Figure 48 shows measured S-parameters and CW large signal results of the PA. The PA has peak S21 of 32.2 dB at 5.5 GHz with a gain variation less than 1.0 dB from 4.9 to 5.9 GHz. Input return loss is higher 10 dB from 4 to 7 GHz and the output return loss is well-matched with the simulation result. Measured output P1dB and saturated P_{OUT} are higher than 32.0 ± 0.4 dBm, and 33.0 ± 0.3 dBm, respectively. Measured AM-PM distortion is within 2.4° at P1dB. Week 2nd and 3rd harmonic emissions of -47dBm/MHz and -80dBm/MHz for 11ac MCS9 VHT80 signal at 100% duty cycle demonstrate the excellent spectral purity of this PA without any harmonic rejection filters.

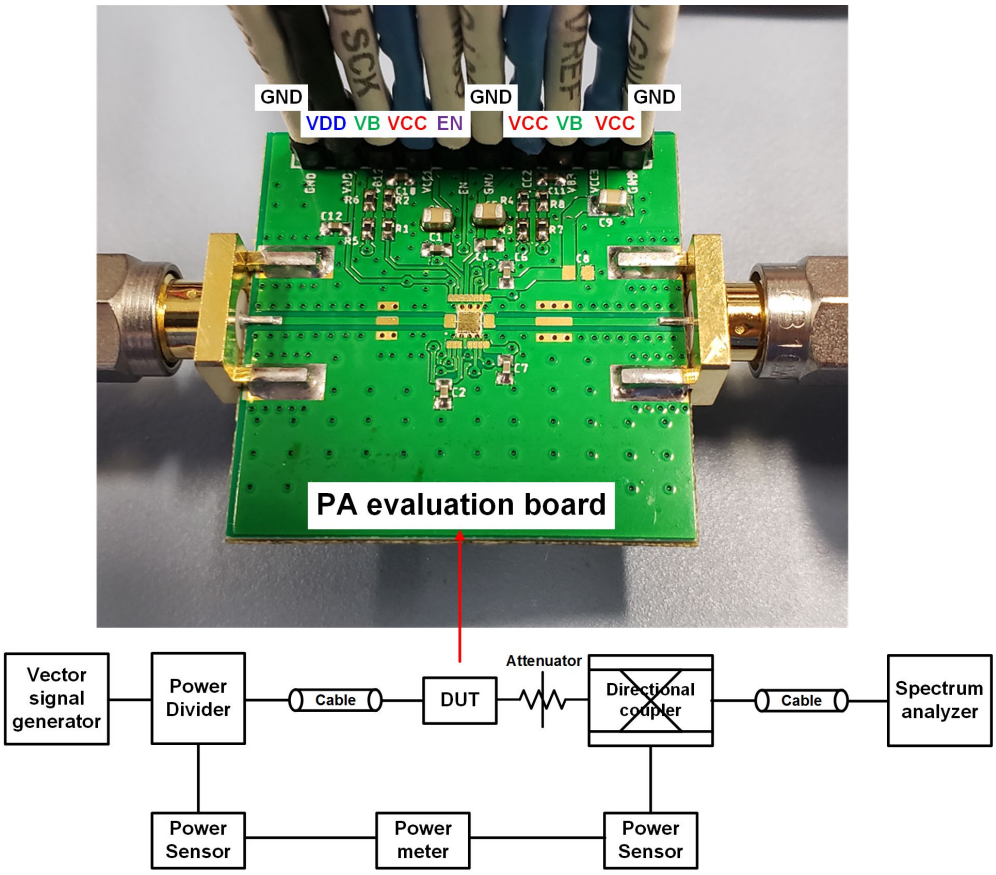


Figure 49 – Fabricated evaluation board (top) and measurement setup (bottom) for DEVM of the PA.

DEVM measurement setup of the PA and its fabricated evaluation board are shown in Figure 49. A vector signal generator synthesizes WLAN standard test signals and dynamic EVM, I/Q constellation, and spectral mask are obtained from a spectrum analyzer. Power sensors, a power meter, and a directional coupler are used to monitor the input and output power precisely. Enable signal from a pulse generator is injected to "EN" port on the PCB to turn on and off the PA for characterizing DEVM. A PA DIE was mounted on a 4-layered PCB using a thermally conductive epoxy EK2000 and all RF and DC pads are wire-bonded to PCB traces. The 4-layered PCB is made of RO 4350B as a top substrate and FR406B as an interposer in the middle and a bottom supporting substrate. No heat sink is put underneath the PCB in the measurement.

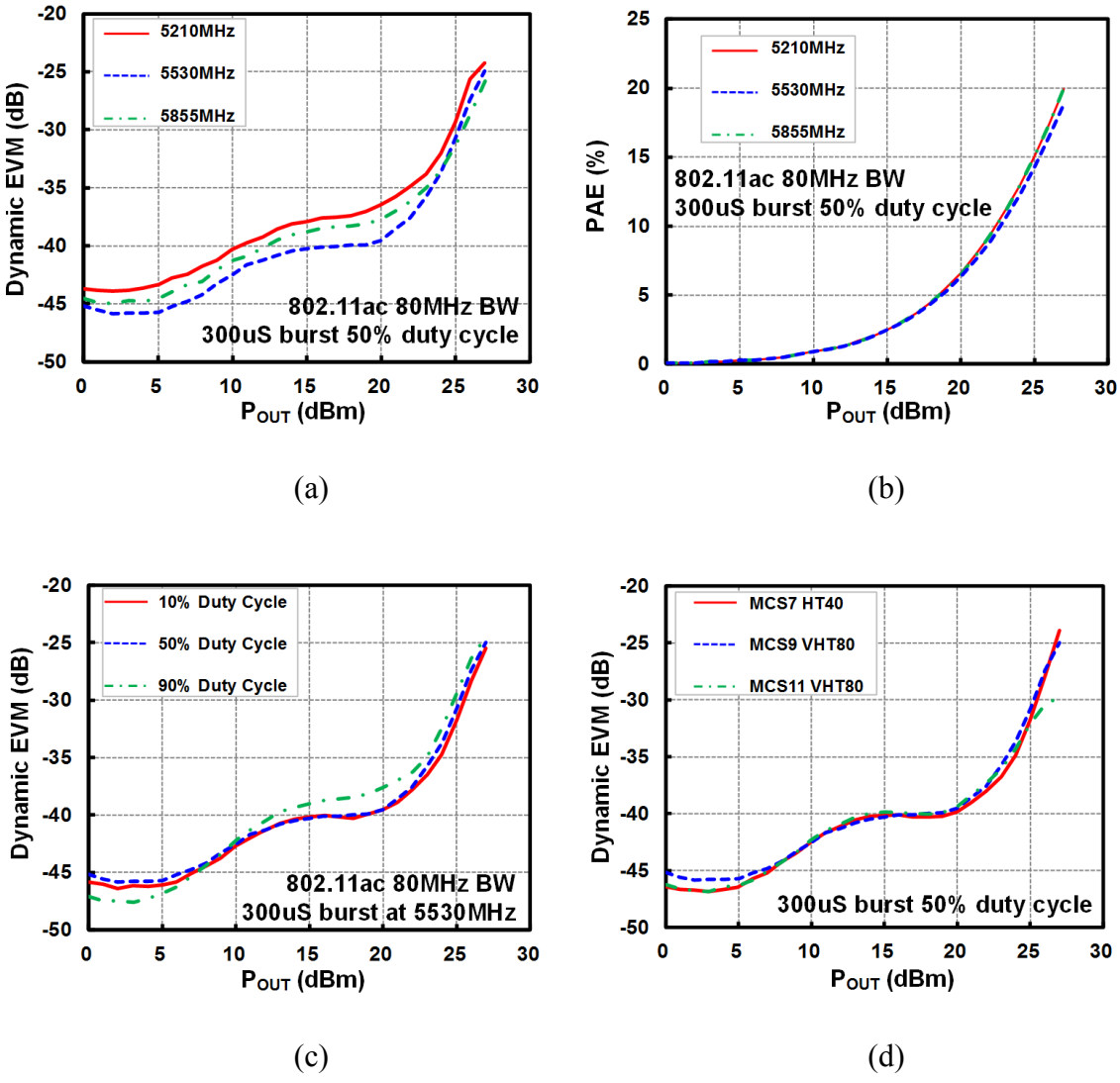


Figure 50 – Measured (a) DEVM for an 802.11ac MCS9 VHT80 signal at 50% duty cycle, (b) PAE, (c) DEVM at various duty cycles at 5530 MHz, and (d) DEVM under several modulations at 5510 MHz for 802.11n MCS7 HT40 and at 5530 MHz for 802.11ac MCS9 VHT80/802.11ax MCS11 VHT80.

Dynamic EVM (DEVM) and PAE of the PA were shown in Figure 50 (a) and (b), respectively. For 802.11ac MCS9 VHT80 signal at 50% duty cycle with the burst length of 300-μs, the PA delivers 22.3, 23.6, and 22.7 dBm P_{OUT} (DEVM=-35 dB) with 10.1, 12.2, and 10.3% PAE at 5210, 5530, and 5855 MHz, respectively. Figure 50 (c) plot shows DEVM result under the various duty cycles (10/50/90%). P_{OUT} (DEVM = -35 dB) higher than 23.1 dBm is observed, which indicates the PA is thermally robust. The PA was also

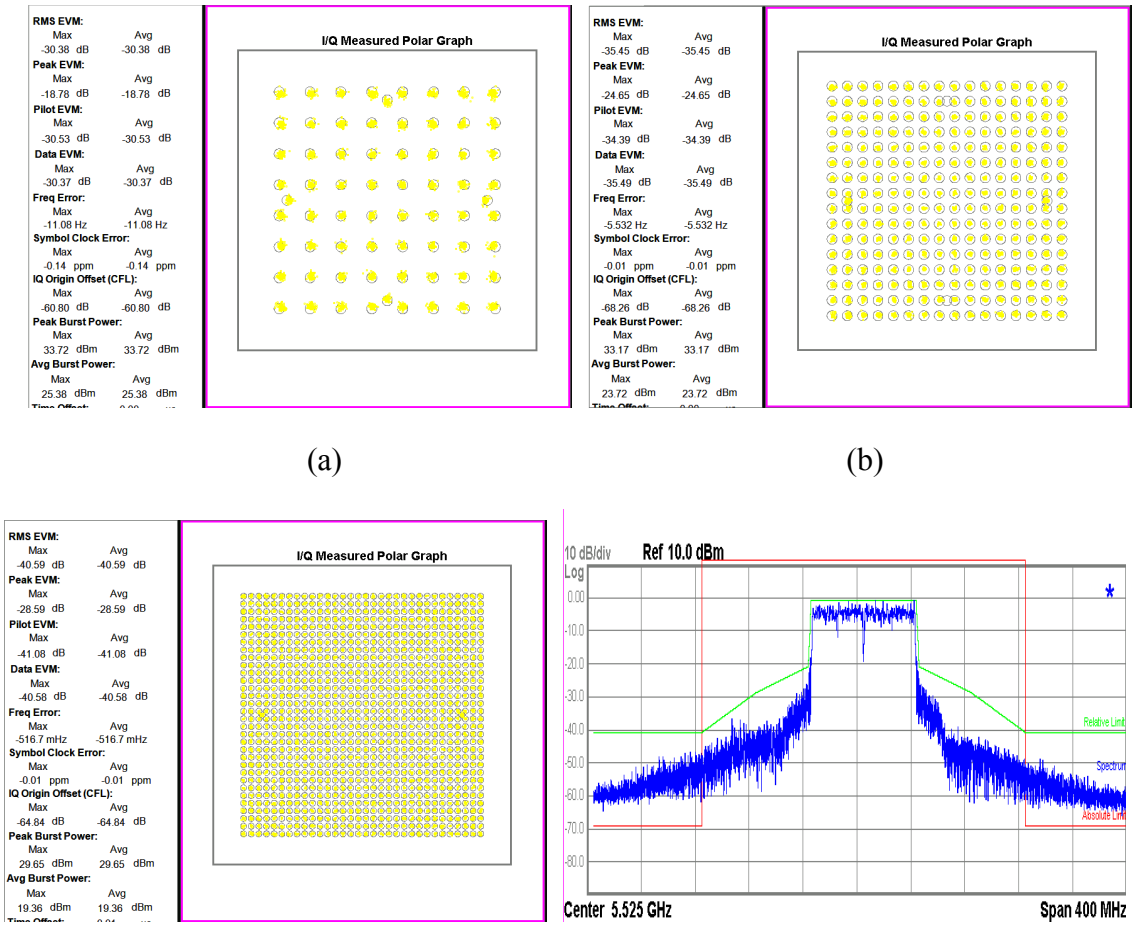


Figure 51 – Measured (a) IQ constellation for 802.11n MCS7 40 MHz test signal, (b) IQ constellation for 802.11ac MCS9 80 MHz test signal, (c) IQ constellation for 802.11ax MCS11 80 MHz test signal, and (d) a spectral mask for 802.11ac MCS90 VHT80 test signal at 5530 MHz and 23.7 dBm.

measured with various modulated signals as shown in Figure 50 (d) and it successfully supports 802.11ax operation (EVM=-38/40dB) at 21.4 and 19.4 dBm. Clear I/Q constellations and a spectral mask are depicted in Figure 51. The PA can modulate 1024QAM signal and passes IEEE spectral mask with 10 dB margin at 23.7 dBm P_{OUT}.

Table 6 summarized benchmarking against prior-art 802.11ac/ax WLAN PAs. The proposed SiGe HBT PA demonstrates the highest linear P_{OUT} and higher or similar PAE compared with Si-based 802.11ac/ax WLAN PAs. It is comparable to III-V GaAs PA.

Table 6 – Comparison of State-of-the-art 802.11ac/ax WLAN PAs

		This work	[96]	[98]	[99]	[103]	[100]	[113]
Technology		SiGe BiCMOS	III-V HBT	55 nm CMOS	40 nm CMOS	SiGe BiCMOS	0.13-μm CMOS	40 nm CMOS
Supported WLAN Standards		11n/ac/ax	11n/ac	11n/ac/ax	11abgn/ac	11n/ac/ax	11ac	11abgn/ac
PA topology		Linear Class-AB	Linear Class-AB	Doherty	Spatial power combining	Linear Class-AB	Linear Class-AB	Linear Class-AB
Frequency (MHz)		4900-5925	4900-5925	4900-5925	4900-5925	4900-5925	4900-5925	4900-5925
Supply (V)		5.0	5.0	3.3	-	5.0	3.6	3.3
Small Signal Gain (dB)		32.2	32.0	26.0	-	32.0	15.0	-
2nd/3rd harmonics (dBm/MHz)		-47/-80	-45/-45	-51/-51	-	-55*/-	-	-
P_{SAT} (dBm)		33	34	29	27	-	26.0	26.0
DPD requirement		No	No	Yes	Yes	No	No	no
11ac MCS9	P_{OUT} (dBm)	23.6	25.0	20.0	16.0/19.0	21.6	16.2	17.0
	PAE (%)	12.2	10.5	12.0**	-	10.2***	8.8	-
	DEVM (dB)	-35	-35	-35	-35	-35	-35*****	-32*****
	Ch. BW (MHz)	80	80	160	80/80+80	80	80	80
11ax MCS11	P_{OUT} (dBm)	21.4/19.4	-	18.0/15.0	-	20.3/19.8	-	-
	PAE (%)	8.5/6.1	-	10.0/7.0**	-	8.4/7.8***	-	-
	DEVM (dB)	-38/-40	-	-38/-40	-	-38/-40	-	-
	Ch. BW (MHz)	80	-	160	-	80	-	-
Chip size (mm^2)		2.03	-	1.42****	-	0.95	-	-

* estimated from S-parameters plot
** DPD power consumption is not included
*** calculated using I_{CC} plot
**** PA balun realized on 0.18µm SOI CMOS is not included
***** Measurement result is static EVM, not dynamic EVM

CHAPTER 6. SPECTRAL PURITY MM-WAVE LO SIGNAL GENERATION USING SIGE HBT FREQUENCY DOUBLER

The rapid growth of data usage in cellular networks is forcing communication standards to move from RF bands to MM-wave bands. Since low phase-noise LO signal generation in MM-wave bands is very challenging, frequency multipliers are frequently used, instead of directly synthesizing LO signal. But designing frequency doublers for 5G communication requires higher output power and high efficiency operation since 5G will include more transmit/receive paths than preexisting 3G/4G communication standards.

Much effort have been made to achieve these goals, including; Gilbert cell frequency doublers [116, 117], single-ended configuration with a output harmonic filter [118, 119], a distributed frequency doubler [120], and balanced frequency doublers [57, 120, 121]. Among those configurations, the balanced frequency doubler is attractive for 5G communication system due to power combining and inherent fundamental frequency rejection ability. Although [121] achieved high power and modest conversion efficiency, it is narrowband and requires an external balun for input feeding. High efficiency and broadband performance were obtained in [121], but its output power and fundamental rejection might be insufficient to feed multiple transmitters and receivers in 5G phased array system.

A high power, highly efficient Ka-band SiGe HBT cascode frequency doubler is proposed. A single foot print four-way input transformer balun is designed to convert a single-ended input signal to two differential signals, with good balance, which helps

improve the output power and fundamental frequency rejection. A cascode configuration with very low base impedance termination is used to boost output voltage swing at 2nd harmonic frequency without catastrophic damage on a SiGe HBT device. In addition, a novel active cell composed of a common-centroid layout configuration of two cascode differential-pairs helps to achieve the record performance of the doubler. This work had been accepted in IEEE Transactions on Microwave Theory and Techniques in 2018 [56].

6.1 Design of A Compact, Highly Efficient High Power SiGe HBT Cascode Ka-Band Balanced Frequency Doubler

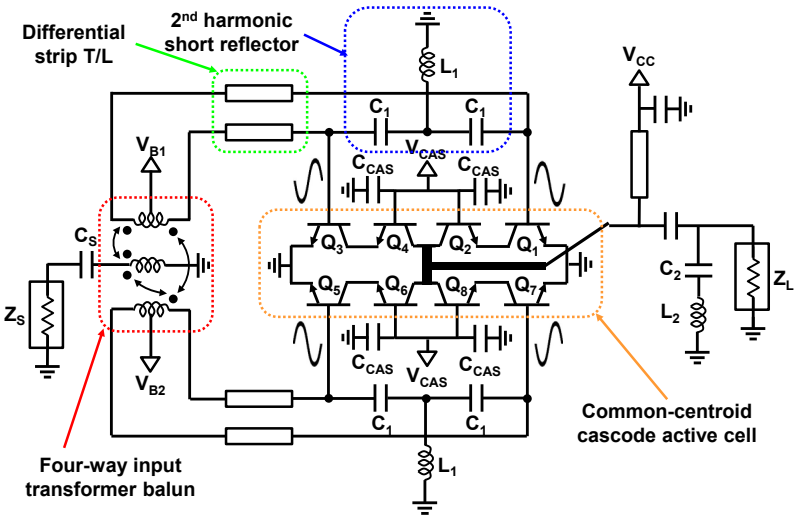
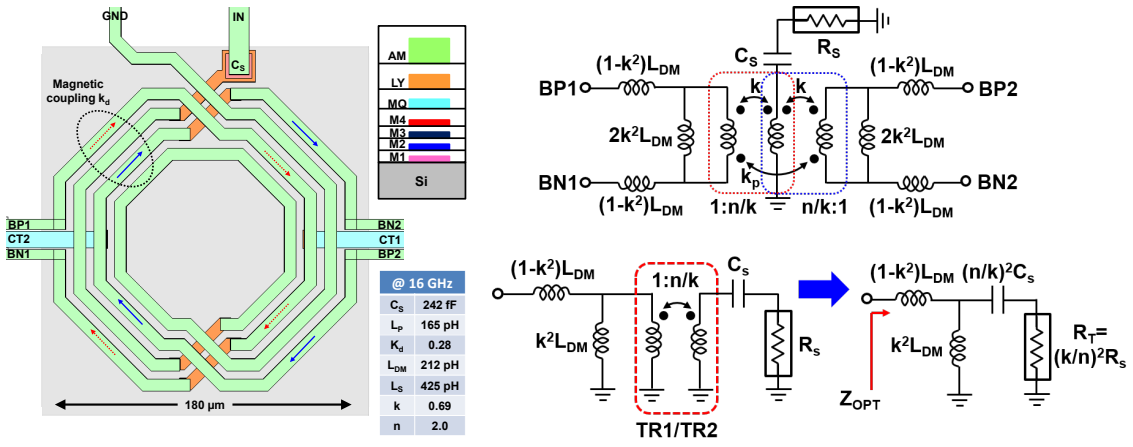


Figure 52 – Circuit schematic of the Ka-band balanced frequency doubler. Each transistor symbol is comprised of two parallel-connected SiGe HBTs.

Figure 52 depicts a circuit schematic of the proposed Ka-band balanced frequency doubler. The main idea is to adopt a novel common-centroid layout configuration for two differential cascode pairs, as highlighted in yellow dotted box in Figure 52. The common-centroid cascode active cell achieves high efficiency, high output power, and strong fundamental rejection as far as differential signals fed to differential cascode pairs maintain their balance. A compact, highly efficient four-way input transformer balun was designed,

not only for converting a single-ended input signal to two differential signals to drive the common-centroid cascode active cell, but also for the impedance transformation between a 50Ω source and each base of common-emitter (CE) HBTs in the cascode. Two differential strip line pairs were inserted between the four-way input transformer balun and the common-centroid cascode cell for simultaneous signal routing and optimum matching.

A 2nd harmonic short reflector [121], frequently used to enhance conversion gain of a frequency doubler, is close to each base of the CE SiGe HBTs. A compact C_1-L_1-C_1 T-network structure is beneficial for minimizing phase mismatch and thereby maximizing conversion gain. The values of L_1 and C_1 are 100 pH and 106 fF, respectively, corresponding to a resonance at 34 GHz. The cascode differential pairs with the 2nd harmonic reflectors attain high conversion gain due to reduced Miller effect and high combined output power from the four cascode cells. While the lower SiGe HBTs in cascode are biased to class B ($V_{B1/B2}$ = 0.75 V) to maximize the 2nd harmonic current, common-base (CB) SiGe HBTs are biased to class AB (V_{CAS} = 1.7 V) to amplify the 2nd harmonic signal efficiently. The simulated quiescent current was 0.9 mA when operated on a 2.5 V. Each CE and CB device in the cascode consists of two parallel-connected SiGe HBTs, with an emitter width and length of 0.12 μm and 9.5 μm, respectively. The total emitter area of the four cascode active cells is 9.12 μm^2. A single collector-base-emitter (CBE) layout SiGe HBT was chosen for both CE and CB SiGe HBTs to simplify routing, reduce emitter degeneration inductance, and realize a compact layout for minimizing phase mismatch at the output. An output matching network was designed to compensate for the narrowband characteristic caused by the 2nd harmonic short reflectors. A series C_2-L_2 resonance tank was inserted at the output network to further suppress fundamental signal leakage.



(a) (b)

Figure 53 – (a) Top view of the proposed four-way input transformer balun and (b) equivalent odd-mode circuit of the four-way input transformer balun (top) and equivalent odd-mode half-circuit of the sub-transformer (TR1/TR2) with the leakage inductance moved to the primary coil (bottom left) and equivalent load at the secondary coil shifted to the primary winding (bottom right).

The design and detailed analysis of the proposed four-way input transformer balun are introduced in this section. Figure 53 (a) depicts a top-view layout of the input transformer. We have also included a simplified cross-section of back-of-end-of-line (BEOL) to clarify its geometry. This input passive network consists of two primary coils and a single secondary coil with a turn ratio n=2. Essentially, two sub-transformers (TR1 and TR2) form a single foot print four-way transformer balun. Since the four-way input transformer balun only needs to handle small magnitudes of base currents, a metal trace width of 7 μm was chosen and the output diameter was just amount 180 μm, which results in a compact size and thus reduced substrate coupling loss. The spacing was determined to be 5 μm to compromise between magnetic coupling strength and lateral capacitive coupling, which is the main cause of imbalance in a differential signal [57]. Each center-tap (CT1 and CT2) of TR1 and TR2 was terminated with a bypass capacitor to help maintain integrity of the differential signal. Comprehensive EM simulations were carried

out using Sonnet®, and the various design parameters of the four-way input transformer are extracted and summarized in the inset table in Figure 53 (a). In odd mode, there is magnetic coupling (denoted as k_P) between the primary coils (TR1 and TR2) as well as that (denoted as k) among the primary coils and the secondary coil. Any current pair on the two primary windings flows in same direction, which leads to magnetic coupling enhancement. As a result, the equivalent primary winding inductance of $L_{DM} = (1+k_P)L_P$ can be obtained, leading to higher quality factor and compact layout. The transformer can be modeled as an ideal transformer with a turn ratio of 1:(n/k), a magnetizing inductance of k^2L_P, and a leakage inductance of $(1-k^2)L_P$ [19]. The equivalent circuit is depicted in Figure 53 (b). It can be further simplified if an equivalent load at the secondary coil is moved to each primary side, as presented in Figure 53 (b).

Simulated impedance at each port (BP1, BN1, BP2, BN2) is plotted in Figure 54 (a). The real and imaginary part of the impedance are within 9.7 ± 1.6Ω and 13.7 ± 1.2Ω over Ka-band and it demonstrates good balance of the four-way input transformer balun. Calculated impedance based on the design parameters and the equivalent circuit is 9.5 + j13.0Ω at 16.0 GHz, very close to the extracted impedance from the simulation. Amplitude and phase imbalance of four differential pairs (BP1-BN1, BP2-BN2, BP1-BN2, BP2-BN1) were also shown in Figure 54 (b) and (c), respectively. Magnitude and phase mismatch are approximately within ±0.7 dB and ±3° from 13 GHz to 20 GHz. Even with the slight imbalance, excellent fundamental rejection was obtained due to the combination of the proposed four-way input transformer balun and the common-centroid cascode active cell. Therefore, it is highly expected that the presented four-way input transformer balun with the common-centroid active cells would achieve inherent odd-mode rejection.

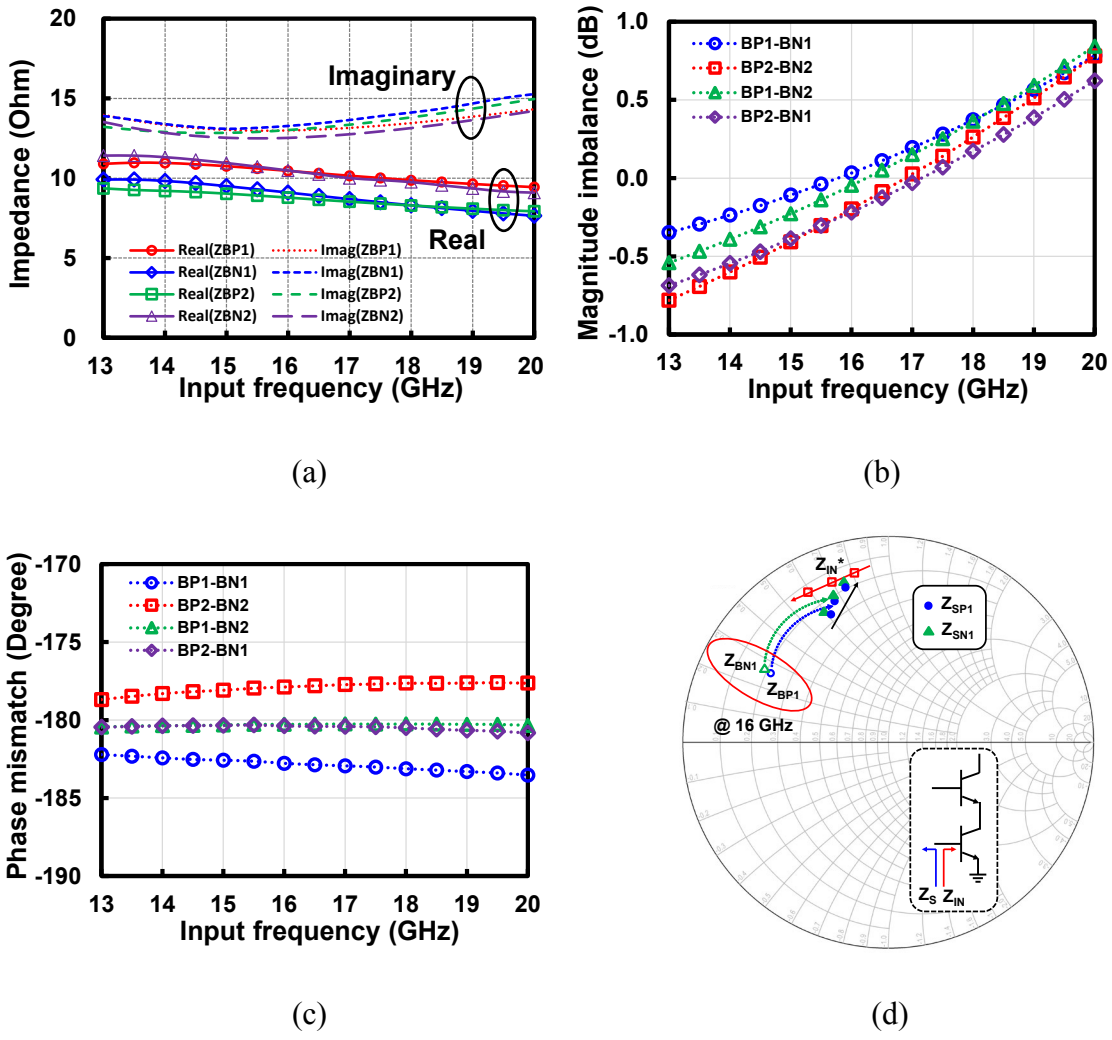
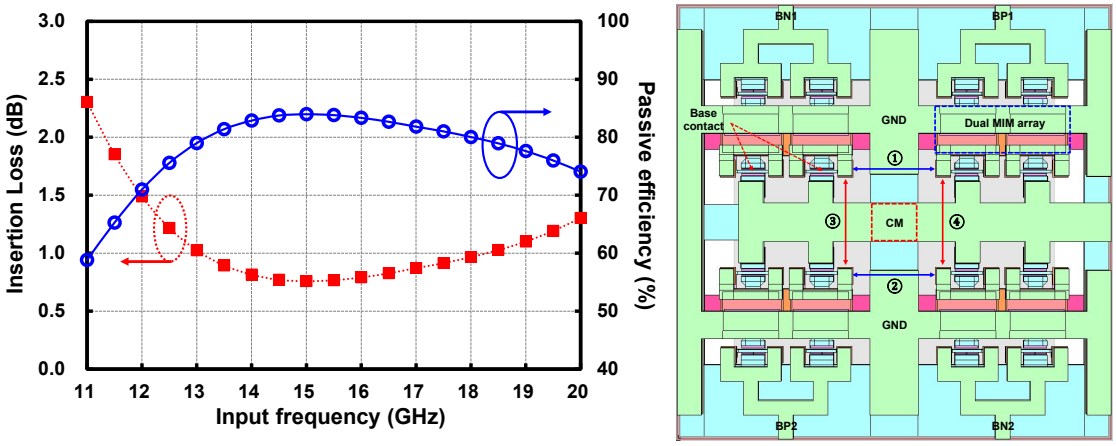


Figure 54 – Simulated (a) real (solid) and imaginary (dotted) impedances of the four-way input transformer balun at BP1, BN1, BP2, and BN2 (b) magnitude imbalance (c) phase mismatch for four differential pairs and (d) impedance loci and their transformation from Z_{BP1} and Z_{BN1} to Z_{IN}*. The source impedances Z_{SP1} and Z_{SN1} at 13, 16, and 19 GHz were plotted with the direction of arrow on solid lines.

The detailed matching process was analyzed with the aid of the Smith chart, as shown in Figure 54 (d). Only impedance loci of Z_{BP1} and Z_{BN1} were depicted because other impedances have similar impedance traces. A simplified cascode circuit schematic in the Smith chart indicates a source impedance of Z_S and an input impedance of Z_{IN} that includes the 2nd harmonic short reflector. The differential strip T/Ls were designed to have Z_{SP1} and Z_{SN1} close to the conjugate input impedance Z_{IN}^* at 16 GHz. The optimization of the

differential strip line has trace width of 7 μm and spacing of 4 μm with MQ layer as bottom ground plane. As Z_S and Z_{IN}^* move in opposite direction to each other with frequency variation, the impedance mismatch at lower frequency is more pronounced than higher frequencies. Nevertheless, the proposed four-way input transformer balun converts the 50Ω source impedance to the optimum impedance of the common-centroid cascode active cell.



(a) (b)

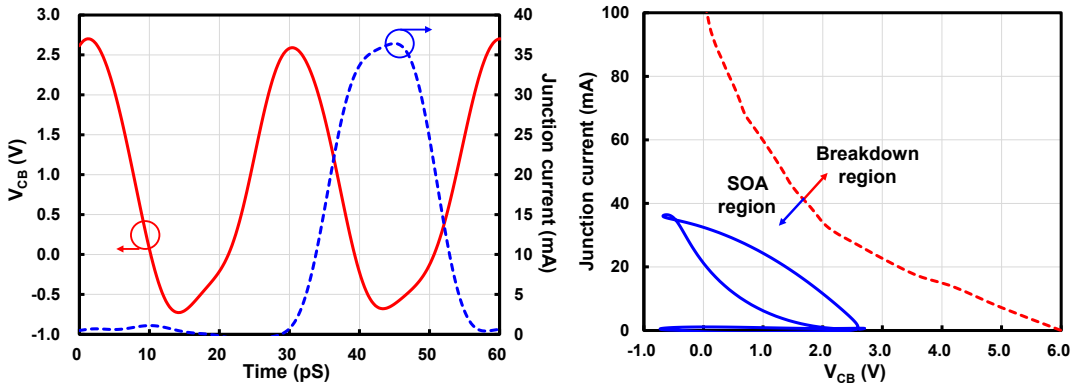
Figure 55 – (a) Simulated insertion loss (rectangular) and passive efficiency (circle) of the four-way input transformer balun and (b) top view layout of the common-centroid cascode cells. Circled numbers indicate the number of differential pairs that suppress fundamental leakage.

Figure 55 (a) plotted simulated passive efficiency and insertion loss of the four-way transformer input balun. The insertion loss of the four-way input transformer balun is lower than 1.3 dB from 13.0 to 20.0 GHz, equivalent to a passive efficiency above 74%. The peak passive efficiency is 84% at 15 GHz (0.7 dB insertion loss) thanks to the positive magnetic coupling between the two primary coils. Thus, the proposed compact four-way input transformer balun can be used for combining the output power from four cascode cells with high conversion efficiency in a small form factor.

The detailed configuration of the novel common-centroid layout for the frequency doubler active cell is shown in Figure 55 (b). It is composed of four cascode cells of which outputs are tied to each other at a common point (denoted as CM) in the layout. Two differential pairs are symmetrically arranged with respect to the common center node, making the frequency doubler robust to process and temperature variation [122]. Using four instances of the fundamental leakage cancellations, as denoted by the circled numbers in Figure 55 (b), helps mitigate imbalance, either caused by the input transformer or mismatch in the cascodes. This is the main advantage of the common-centroid cascode active cell compared with typical balanced topology with a single differential pair since the latter only cancels the fundamental leakage once, and therefore it is sensitive to process variations.

To boost the 2nd harmonic output power while minimizing the contribution of flicker noise and shot noise to the phase noise, the voltage swing at the output should be increased and the current must be decreased simultaneously [52]. Due to the smaller bandgap in Si/SiGe compared to their III-V counterparts, however, Si-based technologies have inherent limitations for high voltage swing operation. Nevertheless, SiGe still has substantially more design headroom than CMOS since its breakdown voltage depends strongly upon base impedance termination and voltage-current waveform overlap [4]. The V_{CB} swing of the SiGe cascode can be extended up to BV_{CBO}, which will greatly improve the voltage swing excursion at the output. Accordingly, base impedance termination of the upper SiGe HBTs in cascode is the most critical design factor for maximizing its voltage swing. To obtain low impedance termination, we propose a dual-layered MIM capacitor array layout scheme. The layout configuration of a cascode cell is shown in Figure 55 (b).

Multi-stacked metal interconnections (M1-M2-M3-M4-MQ) are used to reduce the extrinsic parasitic resistance and inductance at the base contact of the CB SiGe HBT, which in turn alleviates a potential difference on a base stripe and stabilizes high frequency operation of the cascode. The base contacts are then directly connected to a high-quality factor, high density dual-layered MIM capacitor array, which is shown in blue dotted box in Figure 55 (b). Each capacitor value was set to be 0.8 pF to bypass excessive holes generated by impact ionization. The other side of the dual-layered MIM capacitor array was terminated with dual-layered thick top metals (denoted as GND and realized with both AM and LY layers), and thus the parasitic resistance and inductance from the base contact of the SiGe CB HBT to a bypass capacitor ground can be minimized.



(a) (b)

Figure 56 – Simulated (a) transient collector-base junction voltage-current waveforms and (b) dynamic load line, with SOA region indicated as dotted line.

Time domain simulations of a collector-base voltage and a junction current waveform of the CB SiGe HBT are plotted in Figure 56 (a). Simulation was performed for a -1 dBm input power at the input frequency of 17 GHz, with 2.5 V supply. Reduced current-voltage overlap and negligible junction current as V_{CB} swings to a high value indicates that the junction is off at the high end of the voltage swing, and thus it is protected

from pinch-in effects, mitigating damage caused by avalanche multiplication and thermal runaway [64]. The dynamic load line of the collector-base junction voltage and current, together with safe operating area (SOA) region, were plotted in Figure 56 (b). A cascode circuit with ac-grounded bases of the CB SiGe HBTs was utilized to construct the SOA region. The base bias of the CB device is exactly matched with what we used for the frequency doubler design and the only variables here are V_B and V_{CC}. We define a maximum voltage for the circuit to be the point at which an emitter current of the CB device begins increasing rapidly. This is a reasonable assertion since the emitter current can be regarded as a 1st order approximation of a collector-to-base junction current of a CB device [63]. The circuit operation is never beyond the SOA boundary, indicating the proposed SiGe HBT cascode frequency doubler should withstand high voltage swing operation without any catastrophic damage.

6.2 Fabrication and Characterization

The novel balanced cascode Ka-band frequency doubler was fabricated using GlobalFoundries IBM 0.12-μm SiGe BiCMOS technology. This platform offers a single emitter stripe SiGe HBT with f_{max}/f_T of 220/200 GHz at an emitter length of 9.5 μm. Breakdown voltages of a SiGe HBT, represented by BV_{CEO} and BV_{CBO}, are 1.8 V and 6.0-V, respectively. The BEOL features 1 poly layer and 7 metal layers in which a 4 μm thick Al (AM) metal layer is allocated as top metal for low loss passive design. A BEOL resistor, located just on MQ layer, is far removed from the lossy Si substrate, meaning it has smaller parasitic capacitance to substrate than other resistors and thus suitable to be used at higher frequencies. Two types of high quality factor MIM capacitors were provided: a single-layered MIM and a dual-layered MIM. Due to its high density, the dual-layered MIM is

exploited for the bypass capacitor while the single-layered MIM was used for matching purposes in the circuit. Both capacitors are located between the AM and LY layers.

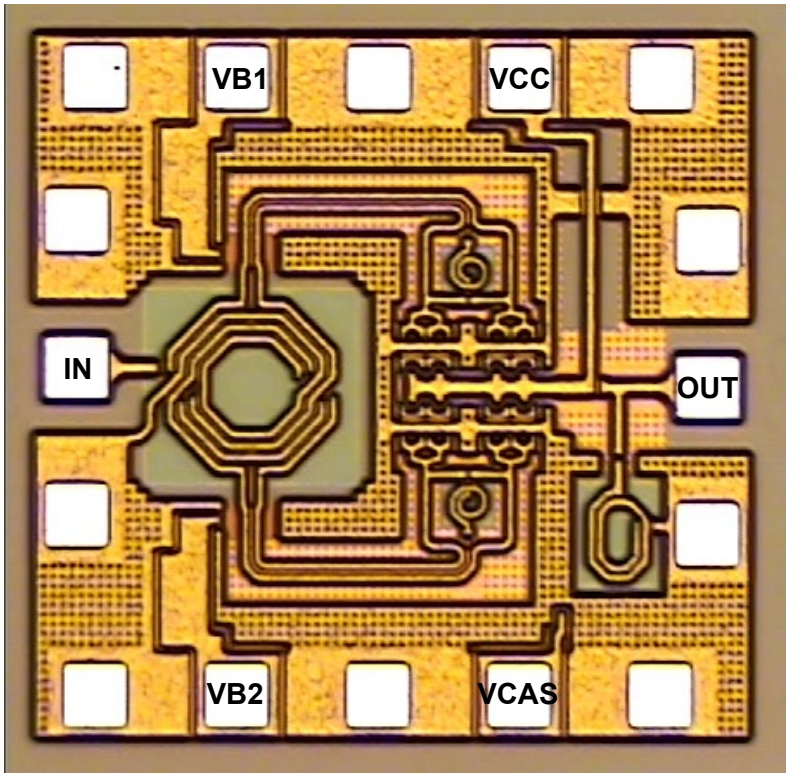


Figure 57 – Microphotograph of the Ka-band balanced SiGe HBT cascode frequency doubler with the four-way input transformer balun.

The chip photograph of the proposed Ka-band frequency doubler is shown in Figure 57. The chip size was 0.74 x 0.68 mm^2 including bond pads. Measurements were performed by using on-wafer probes. Input and output cable losses were carefully compensated by using a signal generator, a power meter, and an on-wafer 200 μm length thru pattern. Output power at the 2nd harmonic frequency was measured using power sensor and power meter. For fundamental output power measurement, however, a spectrum analyzer was utilized since the power meter has a limitation on sensing very low power accurately due to its dynamic range. The fundamental power detected by the spectrum analyzer was then calibrated to the power meter to exactly sense the fundamental leakage.

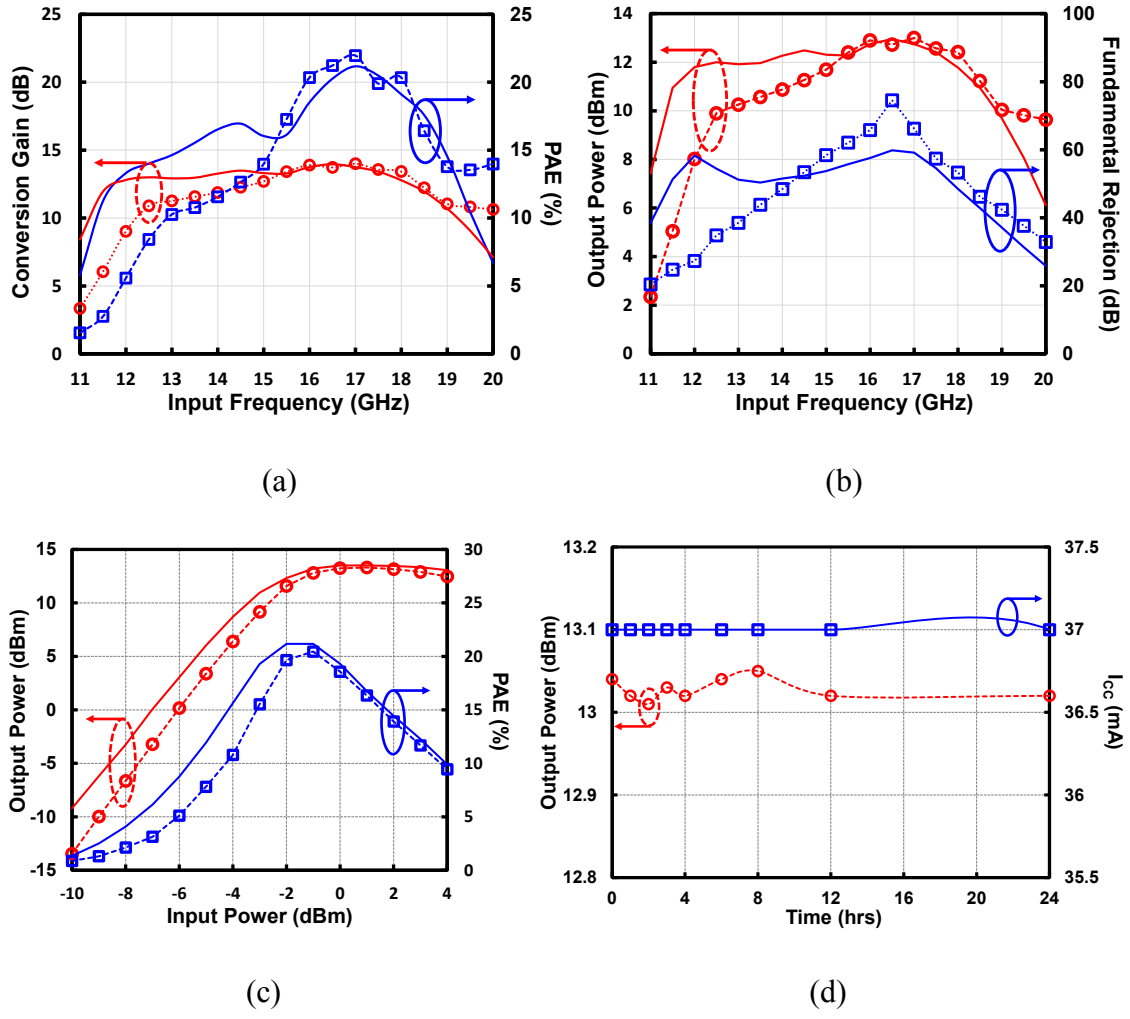


Figure 58 – (a) Measured (symbol) and simulated (solid) conversion gain and PAE at P_{IN} = -1 dBm (b) measured (symbol) and simulated (solid) output power and fundamental rejection at P_{IN} = -1 dBm (c) measured (symbol) and simulated (solid) output power and its corresponding PAE at f_{IN} = 16 GHz and (d) RF stress testing by monitoring the output power (circle) and the supply current (rectangular) for 24 hours (P_{IN} = -1 dBm, f_{IN} = 16 GHz, V_B=0.75 V, V_{CAS} = 1.7 V, and V_{CC} = 2.5 V).

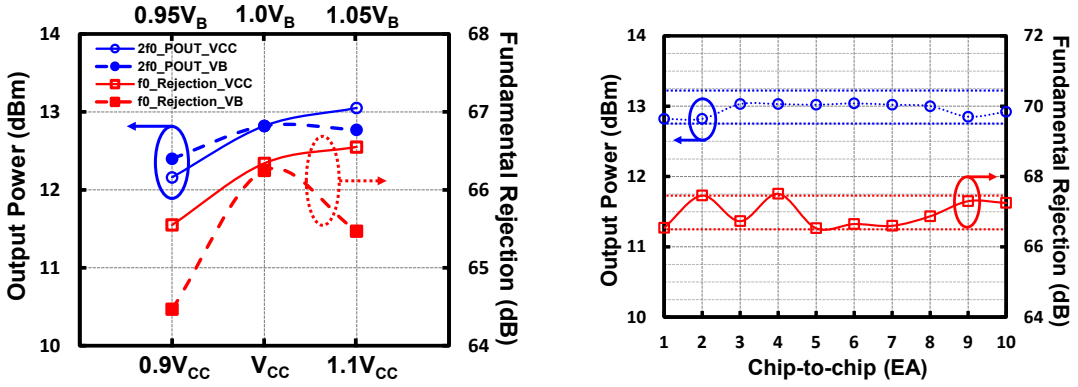
Conversion gain and PAE were measured with input frequency sweep and compared to simulation results in Figure 58 (a). The input power was fixed to -1 dBm. Good agreement between measurement and simulation was confirmed. A slight degradation at lower frequencies may stem from mismatch between simulation and layout, specifically the matching between the four-way input transformer balun and the common-centroid cascode active cell. A maximum conversion gain (CG) of 14.0 dB and peak PAE of 22.0%

at 17 GHz were observed. 3 dB CG bandwidth is from 12.5 to 20.0 GHz, covering the entire Ka-band. The output power (P_{OUT}) and the fundamental suppression are also depicted in Figure 58 (b). The peak P_{OUT} of 13 dBm and the peak fundamental rejection of 74.5 dB at the input frequency of 16.5 GHz were obtained. The fundamental rejection is higher than 35 dB over the Ka-band, which proves that the proposed four-way input transformer balun with the novel common-centroid layout of cascode active cells is beneficial for realizing a spur-free frequency doubler. Figure 58 (c) plotted the P_{OUT} and PAE with input power sweep at 16 GHz. The measured saturated P_{OUT} is 13.5 dBm and the peak PAE is 20.0%, which are in reasonable agreement with simulation.

RF stress testing was carried out by monitoring the output power and the supply current for a continuous 24-h period. It is observed from Figure 58 (d) that no degradation occurs. Longer duration and accelerated tests should be done to guarantee fully reliable operation, but the measurement indicates that the design is robust to high voltage swing.

Mismatch effects, caused by process and supply variations, were also investigated. The output power and the fundamental leakage suppression were monitored with V_{CC} (2.5 ± 0.25 V) and V_B (750 ± 37.5 mV) variations. Only V_{B1} was tuned while V_{B2} is fixed to 0.75 V. It is confirmed from Figure 59 (a) that both output power and fundamental rejection were improved with increases in V_{CC}. V_{B1} mismatch within ±5% induces degradation both in output power and fundamental rejection, but within an acceptable range. We have also performed chip-to-chip measurements for repeatability. Total of 10 chips were measured to see how the output power and the fundamental suppression vary with process. The output power of 12.9 ± 0.1 dBm and the fundamental rejection of 66.9 ± 0.6 dB were observed

from Figure 59 (b), both of which were within or close to the error ranges specified in Figure 59 (b), indicating that the proposed frequency doubler is robust to process variation.



(a) (b)

Figure 59 – (a) Output power and fundamental suppression with V_{CC} (empty symbol) and V_{B1} (solid symbol) variation at P_{IN} = -1 dBm and f_{IN} = 16 GHz and (b) output power (circle) and fundamental suppression (rectangular) with chip-to-chip measurements for P_{IN} = -1 dBm and f_{IN} = 16 GHz.

Because the proposed Ka-band frequency doubler generates more than 10 dBm output power, its current magnitude is not negligible and will have impact on phase noise. The phase noise degradation of a frequency multiplier is given by 20 x log(M), where M is frequency multiplication factor [54]. Based on the equation, any frequency doubler degrades the input phase noise at least by 6 dB at the output. Both input and output phase noise were measured using the spectrum analyzer and the results are plotted in Figure 60. At 10-kHz offset, the input and the output phase noises were -103.32 and -97.20 dBc/Hz, respectively. The measured delta phase noise, which is the output phase noise subtracted from the input phase noise plus 20 x log(2), is within ± 1.0 dB from 1.5 kHz to 1 MHz, indicating the proposed high power and high efficiency Ka-band frequency doubler is immune to phase noise. The phase noise addition below 1 kHz offset would stem from the flicker noise (1/f noise) generated by cascode active cells.

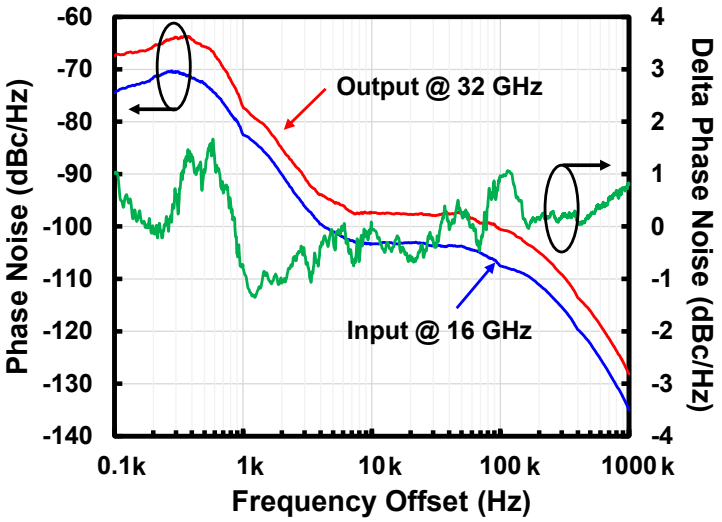


Figure 60 – Measured phase noise for the input frequency of 16 GHz (Blue), the output frequency of 32 GHz (Red), and the delta phase noise (Green) for P_{IN} = -1 dBm.

Finally, published state-of-the-art Ka-band frequency doublers were summarized in Table 7. Our work shows the highest PAE, the highest output power/conversion gain without output buffers, the highest output power density, and higher or comparable fundamental rejection among any frequency doubler. Those performances are even better than III-V GaAs frequency doublers. A doubler figure-of-merit (FOM) has been calculated for performance comparisons and Equation 21 is shown as below

$$\text{FOM} = \left[10log\left(\frac{100 \cdot P_{OUT,2f0}}{P_{IN,f0}+P_{DC}}\right) + FR\right] \cdot BW \tag{21}$$

where $P_{OUT,2f0}$ is the output power at 2nd harmonic frequency, $P_{IN,f0}$ is the input power at fundamental frequency, P_{DC} is the power dissipation, FR is the fundamental rejection, BW is 3 dB fractional conversion gain bandwidth, and CG is peak conversion gain of the frequency doubler. The calculated FOM is 22.4, which is either higher (better) or comparable to other published work. We note, however, that for many emerging

applications (e.g., 5G), this well-established doubler FOM depends too strongly on bandwidth itself, not the gain-bandwidth product. As a result, relying only on this FOM for frequency doubler assessment may be inappropriate, and a new FOM that takes conversion gain and PAE of frequency doublers into account should be considered. The present doubler significantly outperforms other published work when these other parameters are taken into consideration. As such, the proposed novel balanced SiGe HBT cascode frequency doubler with the four-way input transformer balun and the common-centroid layout configuration should be a promising solution to provide 5G transmit/receive elements phased arrays with a high power LO signal efficiently.

Table 7 – Comparison of State-of-The-Art Ka-Band Frequency Doublers

Reference	[116]	[117]	[118]	[119]	[121]	[123]	[124]	[125]	[126]	[127]	**[56]**
Technology	0.4-µm SiGe BiCMOS	0.25-µm SiGe BiCMOS	90-nm SOI CMOS	0.5-µm GaAs pHEMT	0.8-µm SiGe BiCMOS	0.12-µm SiGe BiCMOS	0.18-µm SiGe BiCMOS	0.18-µm bulk CMOS	0.2-µm GaAs pHEMT	0.18-µm bulk CMOS	**0.12-µm SiGe BiCMOS**
Topology	Differential Gilbert-cell	Single-Gilbert-cell	Single-output filter	Single-Dual-gate	Differential-Balanced	Single-Balanced	Single-Balanced	Single-Balanced	Single-Balanced	Single-Balanced	**Single-Balanced**
Frequency (GHz)	22.0-38.0	22.0-30.0	27.0	36.0-41.6	34.6-37.6	27.0-41.0	26.0-40.0	15.0-36.0	4.0-42.0	25.0-75.0	**25.0-40.0**
P_{OUT} (dBm)	0.0	-7.0	-3.0	7.0	10.5	8.0	5.0	-5.2	6.0	-0.7	**13.0**
Peak η / PAE (%)	0.5 / -	0.3 / -	5.0 / 1.5	20.0 / -	9.8 / 6.4	18.0 / 16.9	4.8 / -	2.7 / -	0.7 / 0.5	-	**22.9 / 22.0**
Conv. Gain (dB)	8.6	-6.0	1.5	-0.9	4.5	12.0	-5.0	-10.2	6.0	-11.0	**14.0**
3 dB BW (%)	53.3	30.8	7.4	14.4	13.0	41.2	42.4	82.4	165.0	100.0	**46.2**
Fund. rejection (dB)	> 15.0	> 30.0	> 11.0	> 15.0	> 35.0	> 25.7	> 14.0	> 33.0	> 15.0	> 32.0	**> 35.0**
P_{DC} (mW)	185	65	10	25	114	35	66	11	600	0	**87**
Chip size (mm^2)	0.25	0.35	0.10	1.0	0.54	0.34	0.56	0.32	3.0	0.24	**0.50**
Power density (mW/ mm^2)	4.00	0.57	5.00	5.00	20.78	18.56	5.64	0.94	1.33	3.55	**40.00**
FOM	6.6	7.6	1.3	3.9	5.8	15.7	8.6	29.9	21.8	40.6	**22.4**

CHAPTER 7. CONCLUSION

7.1 Summary of Works

This study suggests several circuit design techniques for SiGe HBT power amplifiers not only by relying on the circuit design perspective, but also thorough the deep understanding of the large signal characteristic of the SiGe HBT devices. The optimized design strategy, which is applied to specific applications, provides several advantages including: meeting highly efficient operation of the SiGe HBT PAs, the co-design method between transmit and receive modes in the SiGe BiCMOS FEM, more than one octave bandwidth achievement in the distribute power amplifier, the highly linear WLAN PA with the optimal electro-thermal design, and the combined active and passive design scheme for the spectral purity MM-wave frequency LO signal synthesis. These benefits prove the potential of SiGe HBT BiCMOS technologies for developing low cost, highly integrated power amplifier. The specific contributions of this work as below:

1. The analysis and design of the two novel passives for synthesizing impedances to support inverse class-F mode of operation. The high efficiency is attained thanks to the voltage excursion capability of the SiGe HBT cascode with the low base impedance termination, which is never achieved in CMOS cascode PA. The output power of 25.6 dBm with the peak PAE higher than 50% at 10 GHz will be the record performance among any Si-based X-band power amplifiers.
2. Set the co-design methodology between the asymmetric CMOS SPDT and the SiGe HBT cascode LNA to obtain the insertion loss of 1 dB and the output P1dB of 0.5W in transmit mode while 15 dB gain with the lowest noise figure of 1.9

dB in receive mode. Such optimization is the unique advantage that SiGe HBT process offers, compared with only CMOS technology.

3. Developing the compact, lumped-element Wilkinson power divider/combiner (WPDC) which covers from 5 to 19 GHz bandwidth with the insertion loss less than 1 dB and isolation better than 10 dB. The concept of this work is extended and then applied to the SiGe HBT cascode non-uniform distributed power amplifier. The proposed design method achieves the peak output power of 24.2 dBm at 7 GHz, with the 3 dB bandwidth from 2 to 19 GHz. The eye-diagram measurement indicates that the non-uniform DPA would be promising for developing multi-purpose wideband applications.
4. The design of the highly linear, high power SiGe HBT power amplifier using the novel built-in 2nd harmonic-shorted four-way output transformer balun and the thermally-compensated dynamic bias circuit with the integrated temperature sensors for linear operation. Its peak linear output power is 23.6 dBm at 5530 MHz with PAE of 12.2% for 802.11ac VHT80 signal (50% duty cycle and 300 uS long burst). The PA also successfully supports 802.11ax operation meeting EVM of -38 and -40 dB at 21.4 and 19.4 dBm output power, respectively.
5. The Ka-band SiGe HBT cascode frequency doubler for the emerging 5G application. The novel common-centroid active cell and the compact four-way input transformer balun enable to obtain the output power of 13 dBm with PAE of 22% without any output buffer and its 3 dB bandwidth entirely covers Ka-band. The 6 dB degradation in the phase noise would be clear advantage in synthesizing spectrally-cleaned LO signal, compared to the direct LO generation.

7.2 Future Works

1. Even though the proposed X-band inverse class-F PAs demonstrated the highest PAE at sub-Watt level, there is still increasing demand on developing a truly Watt level Si-based X-band PA. Using a four-way transformer balun with the waveform engineering would be possible to achieve the goal.
2. To support Watt-level SiGe HBT X-band PAs, the X-band FEM should be sustainable Watt-level power in transmit mode. In order to achieve that, a series switch in the transmit path must be removed and a sufficient isolation from the antenna port to the PA output should be guaranteed not to affect the noise figure. It would be worth designing a higher Q pi network using an advanced Cu BEOL option for better isolation from the transmit path to the LNA.
3. Replacing a bulky and expensive external bias tee with a small footprint on-chip RF choke will be necessary for the implementation of a low cost and broadband SiGe HBT distributed PA. Stability of the amplifier will be the most important concern when the on-chip RF chokes are used in the SiGe HBT DPA. Therefore, more conservative design perspective must be taken for SiGe HBT cascode power cells. For example, multiple resistors at the base and/or the emitter of SiGe HBTs in the cascode would help to quench a low frequency oscillation, a high frequency oscillation, and a parametric oscillation. Of course, the value of the resistors should be chosen carefully not to degrade RF performance of the PA.
4. DEVM of the highly linear SiGe HBT PA for 802.11ax WLAN test signal can be improved further not only through the optimization of passive matching networks, but also by designing PTAT current source in the driver stage to

compensate for the gain variation caused by the electro-thermal transient response. The optimized power cell arrangement with different emitter ballasting resistors would improve the performance of the PA further.

5. Extension of the proposed Ka-band frequency doubler to a quadrupler will be the next target. Suitable arrangement of SiGe HBT cascode power cells in combination with a lumped-element quadrature hybrid would be one solution in realizing a compact, highly efficient, and high power MM-wave frequency quadrupler without any output buffer and harmonic rejection filters.

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